



*TOMORROW  
starts here.*

Cisco *live!*



# Cisco Enterprise Silicon – Delivering Innovation for Advanced Routing and Switching

BRKARC-3467

Rohan Saldanha - Systems Engineer

#clmel

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# Cisco Enterprise Silicon

Delivering Innovation for Advanced Routing and Switching

## BRKARC-3467 – Session Overview and Objectives

**Come to this session to learn about the latest advances in Cisco Enterprise silicon development – ASIC (Application Specific Integrated Circuit) hardware which provides a key foundational element of the Cisco ONE Enterprise Architecture, and which support key industry trends such as SDN.**

**Attendees at this session will gain a greater insight into how ASICs are created, showcasing the advanced capabilities and functionality delivered by two of Cisco's latest switching and routing silicon innovations UADP (Unified Access Data Plane) and QFP (QuantumFlow Processor).**

By developing custom silicon, and leveraging this advanced hardware within our Enterprise portfolio, Cisco has always provided differentiating capabilities and compelling customer value across many platforms.

In this session, we will **explore the capabilities and advantages** provided by custom Cisco silicon, **provide greater insight** into the functionality delivered by existing Cisco Enterprise ASICs, and **explore the new capabilities and solutions** enabled by Cisco's latest generation of Enterprise-focused programmable switching and routing chipsets – UADP and QFP.

# Agenda

- Why ASICs?
- How is an ASIC Developed?
- Merchant vs. Custom
- Cisco ASIC History
- The Move to Programmability
- QFP
- UADP
- Summary

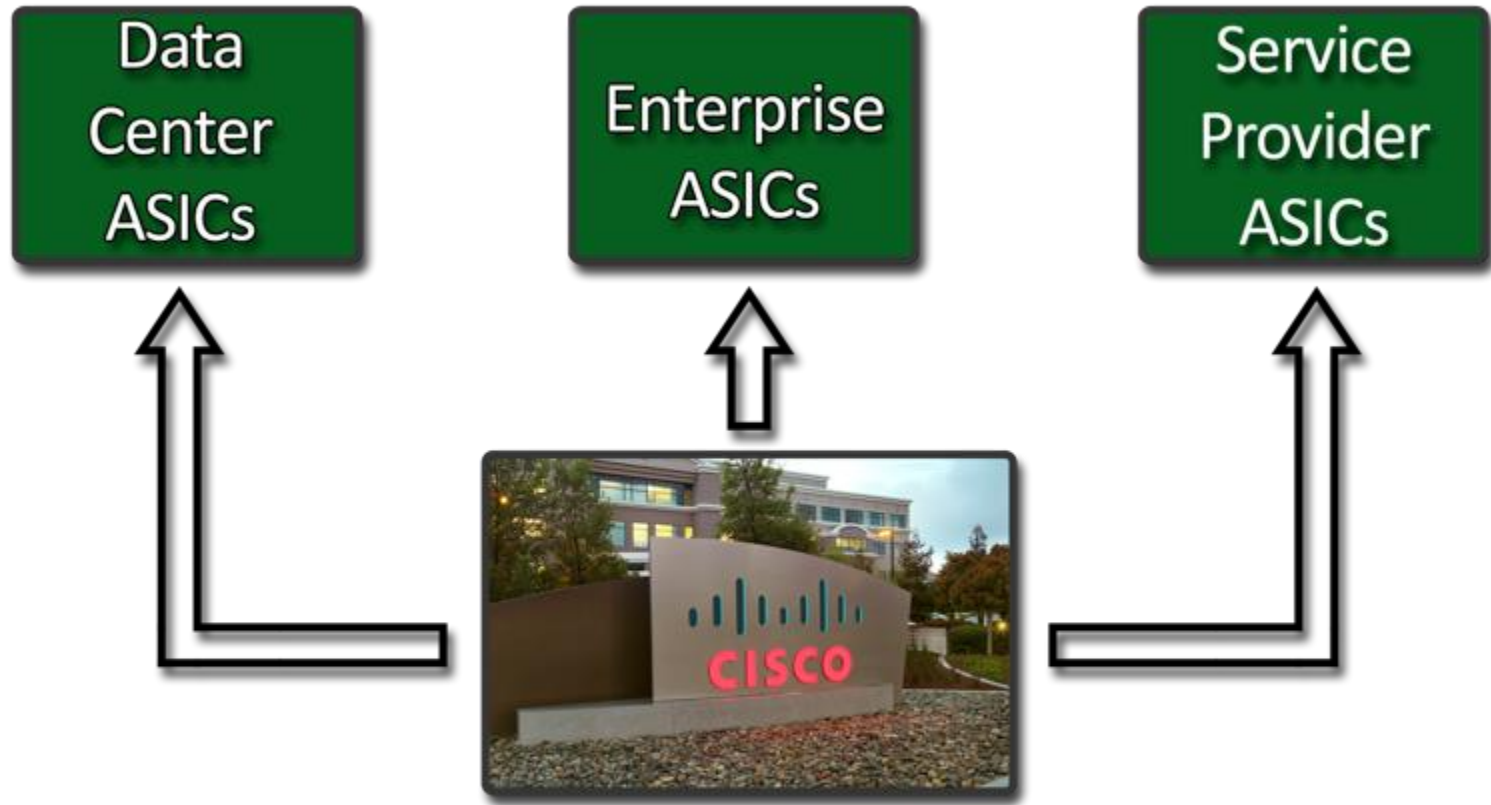




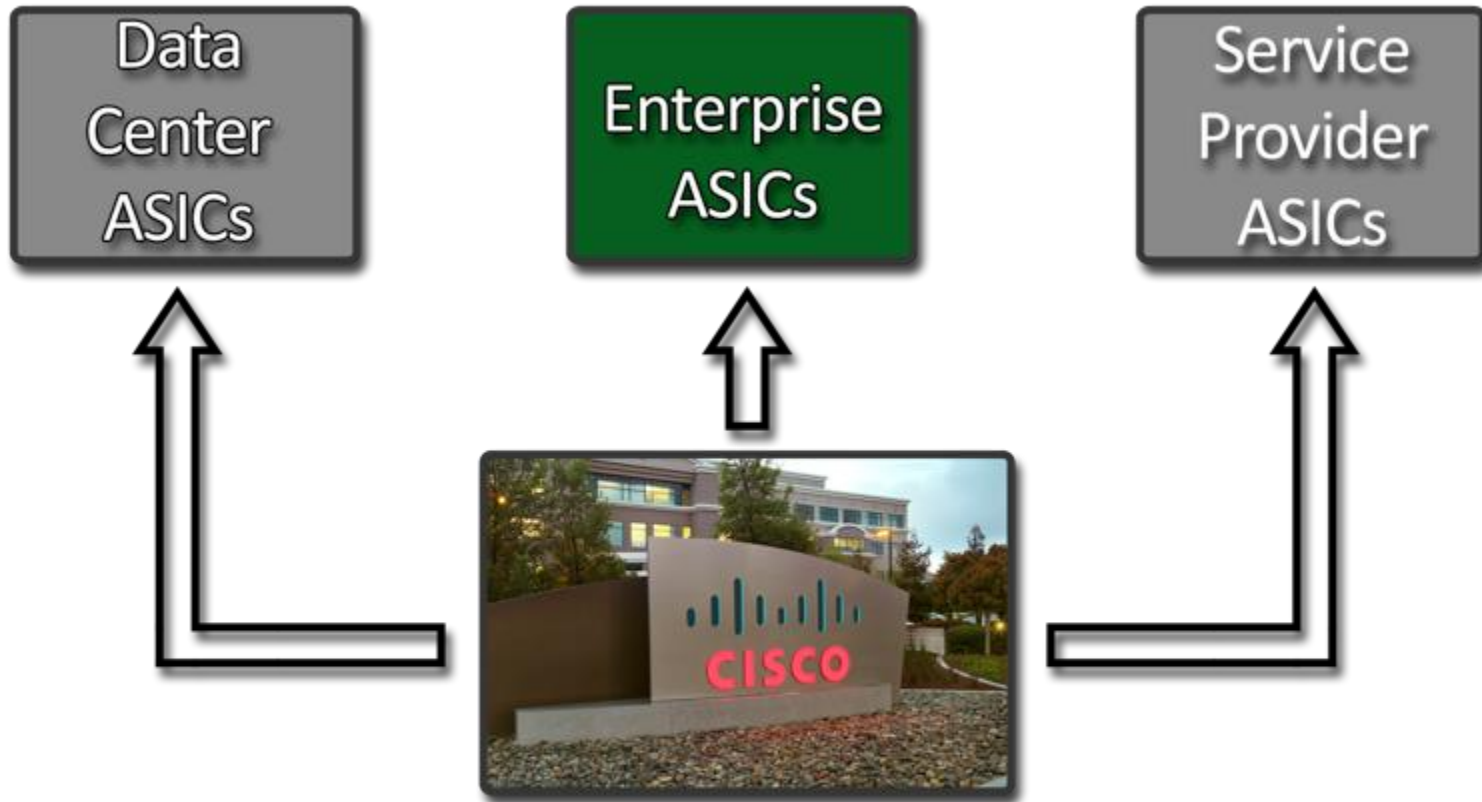
# What is an ASIC?

---

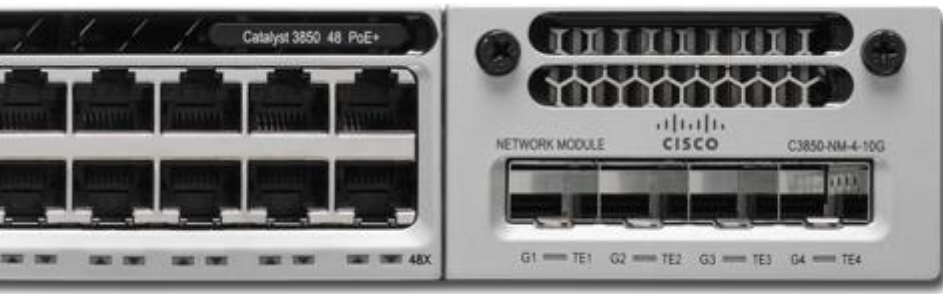
“An *Application Specific Integrated Circuit* is an integrated circuit customised for a particular use, rather than intended for general purpose use...”



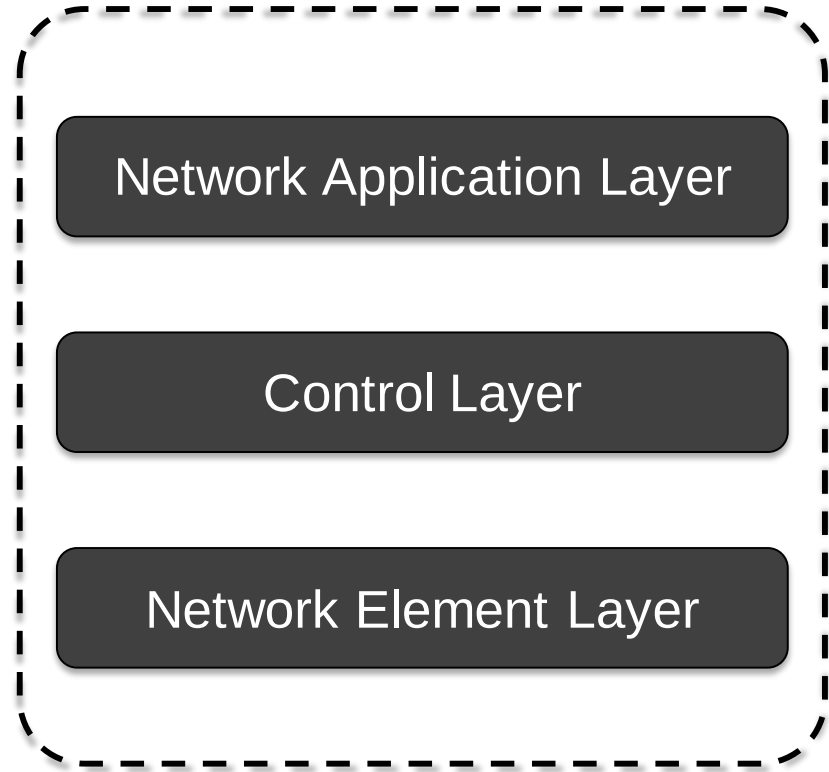
Cisco has a wide portfolio of ASICs

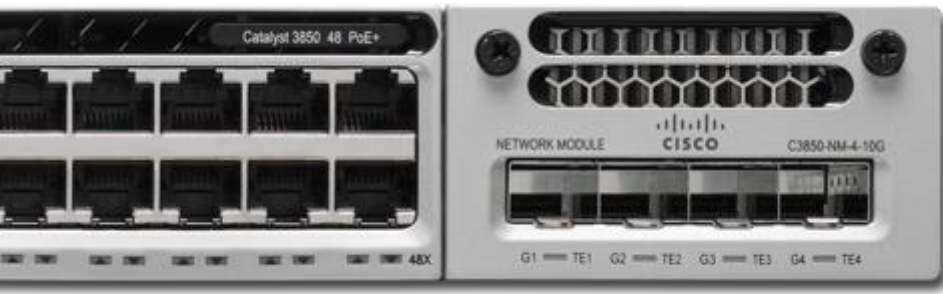


This presentation focuses on Enterprise Network ASICs only



# Enterprise Architectural Template





## Where ASICs Play...

Network Application Layer

Control Layer

Network Element Layer

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# How is an ASIC built?



Marketing



Engineering



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Then, it starts with coding...

Verilog  
VHDL

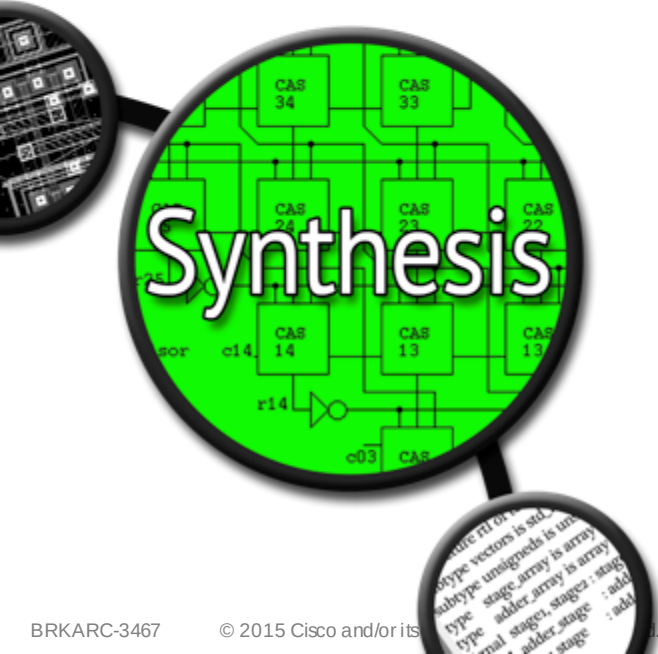
RTL

RTL – Register Transfer Level

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# Synthesis Process

Converts code into  
logical gate constructs (Netlist)

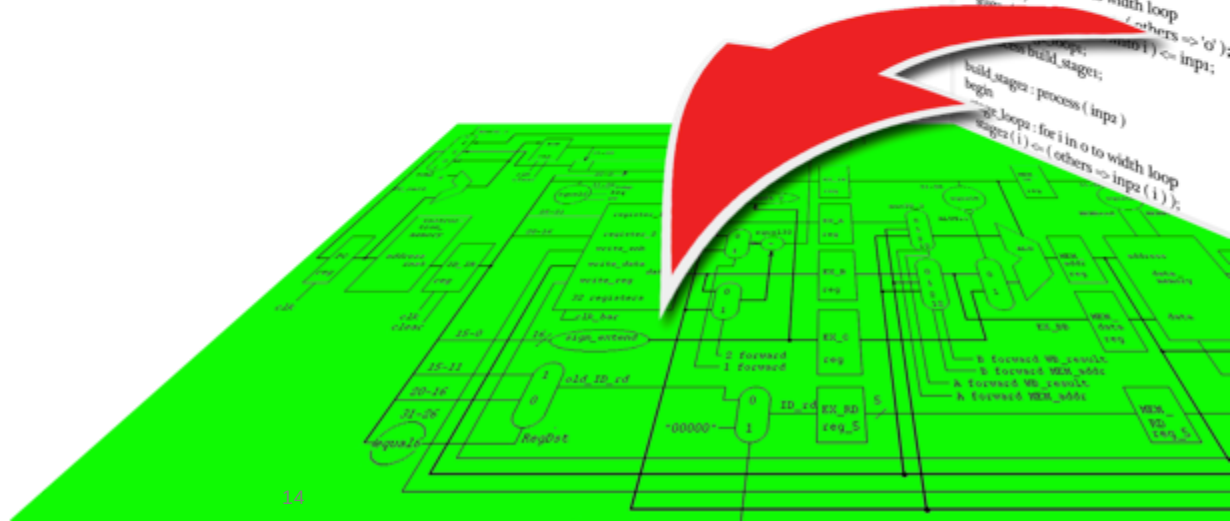


```
port ( clk      : in std_ulogic;  
      reset    : in std_ulogic;  
      enable   : in std_ulogic;  
      inps, inpa : in std_logic_vector ( width downto 0 )  
      sum      : out std_logic_vector ( width * 2 )  
end test_multipe;
```

```
architecture rtl of test_multipe is  
  subtype vectors is std_logic_vector ( ( width * 2 )  
  subtype unsigneds is unsigned ( ( width * 2 )  
  type stage_array is array ( width downto 0 )  
  type adder_array is array ( width downto 0 )  
  signal stages, stages2 : stage_array;  
  signal adder_stage     : adder_array;  
  signal reg_stage       : adder_array;  
begin -- rtl
```

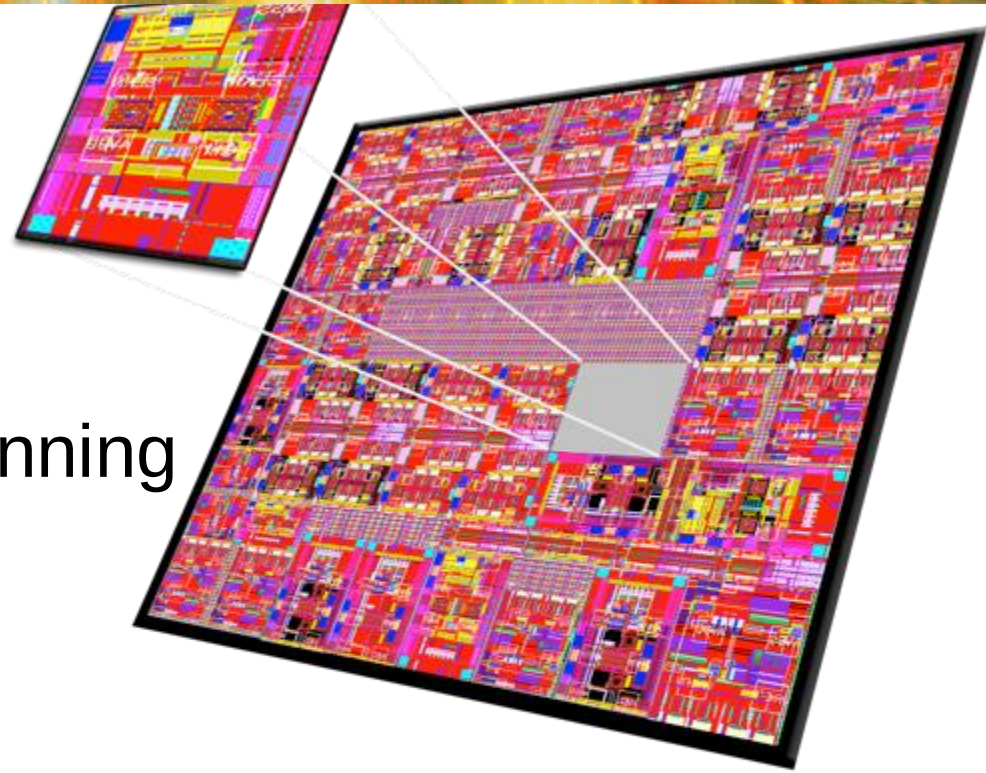
```
-- Fill the two arrays  
build_stages : process ( inps )  
begin  
  stage_loops : for i in 0 to width loop  
    stages ( i )  
    stages2 ( i )  
  end loop  
end build_stages;
```

```
-- Fill the two arrays  
build_stages : process ( inps )  
begin  
  stage_loops : for i in 0 to width loop  
    stages ( i )  
    stages2 ( i )  
  end loop  
end build_stages;
```



# Floor Planning & Placement

Floor planning



Placement

Arrange and interconnect constructs, connect power, minimise crosstalk, etc...

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# Imprint design on Silicon Wafer

Light Source

Photo  
Masking

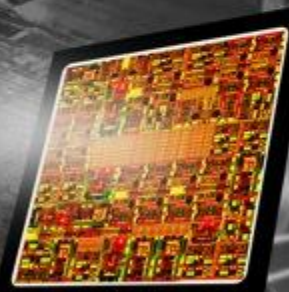


Photo  
Mask

Silicon  
Wafer



# Validation of Chip functionality

The background of the slide is a grayscale image of a silicon wafer, showing a grid of individual chips. A gloved hand is visible on the right side, holding a magnifying glass that focuses on one of the chips. The overall theme is semiconductor technology and quality control.

Testing  
Packaging

A circular inset in the lower-left corner shows a close-up of a green printed circuit board (PCB) with various electronic components. The text "Testing Packaging" is overlaid on this image in a white, sans-serif font.



Some manufacturing considerations...



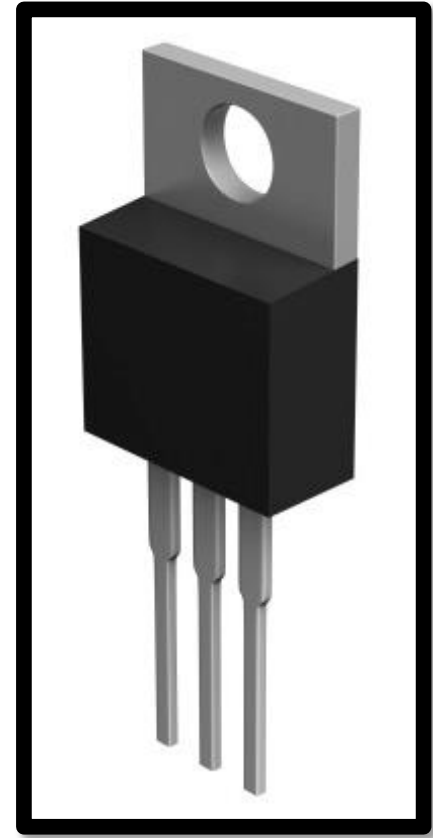
Sometimes we question  
if size matters??



In the ASIC world  
the **smaller** the better!

# We are talking transistors...

and how many we can pack  
in an ASIC die ...



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**Gordon Moore**



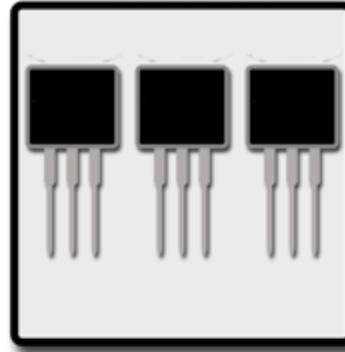
“The number of transistors incorporated into a chip will approximately double every 24 months ...”

“Moore’s Law” - 1975

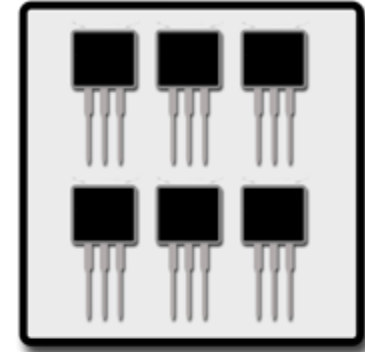
# Transistor Width measured in Nanometers



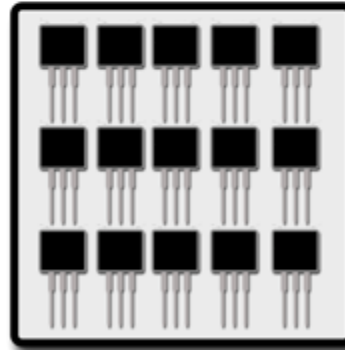
65nm



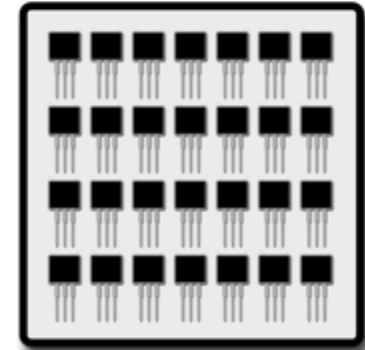
45nm



Nanometer = One Billionth of a Meter



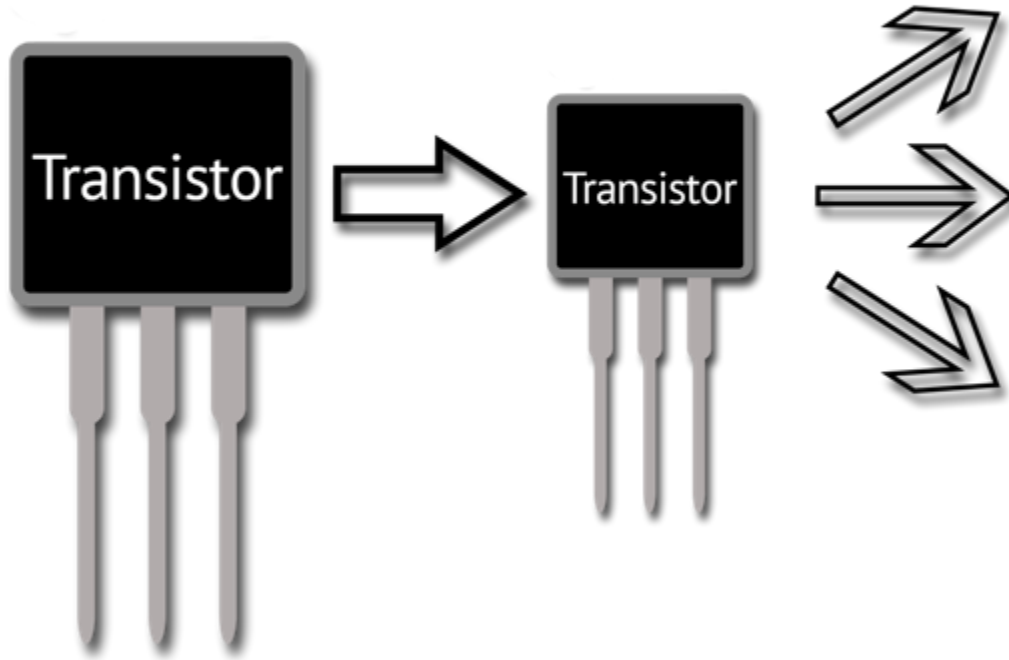
32nm



22nm

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# Use of smaller technology leads to benefits ...



Lower Price

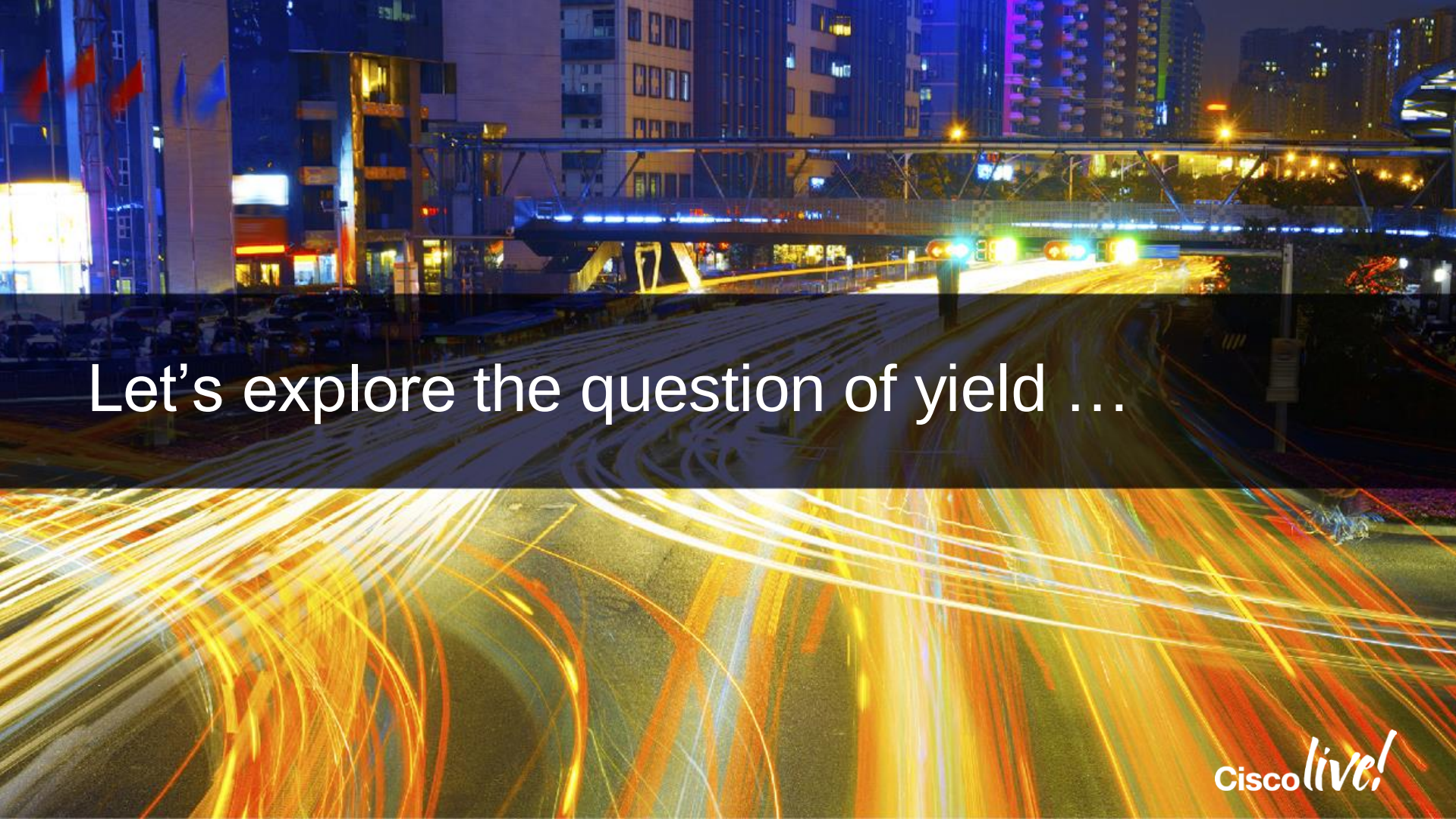


Lower Power



Higher  
Performance

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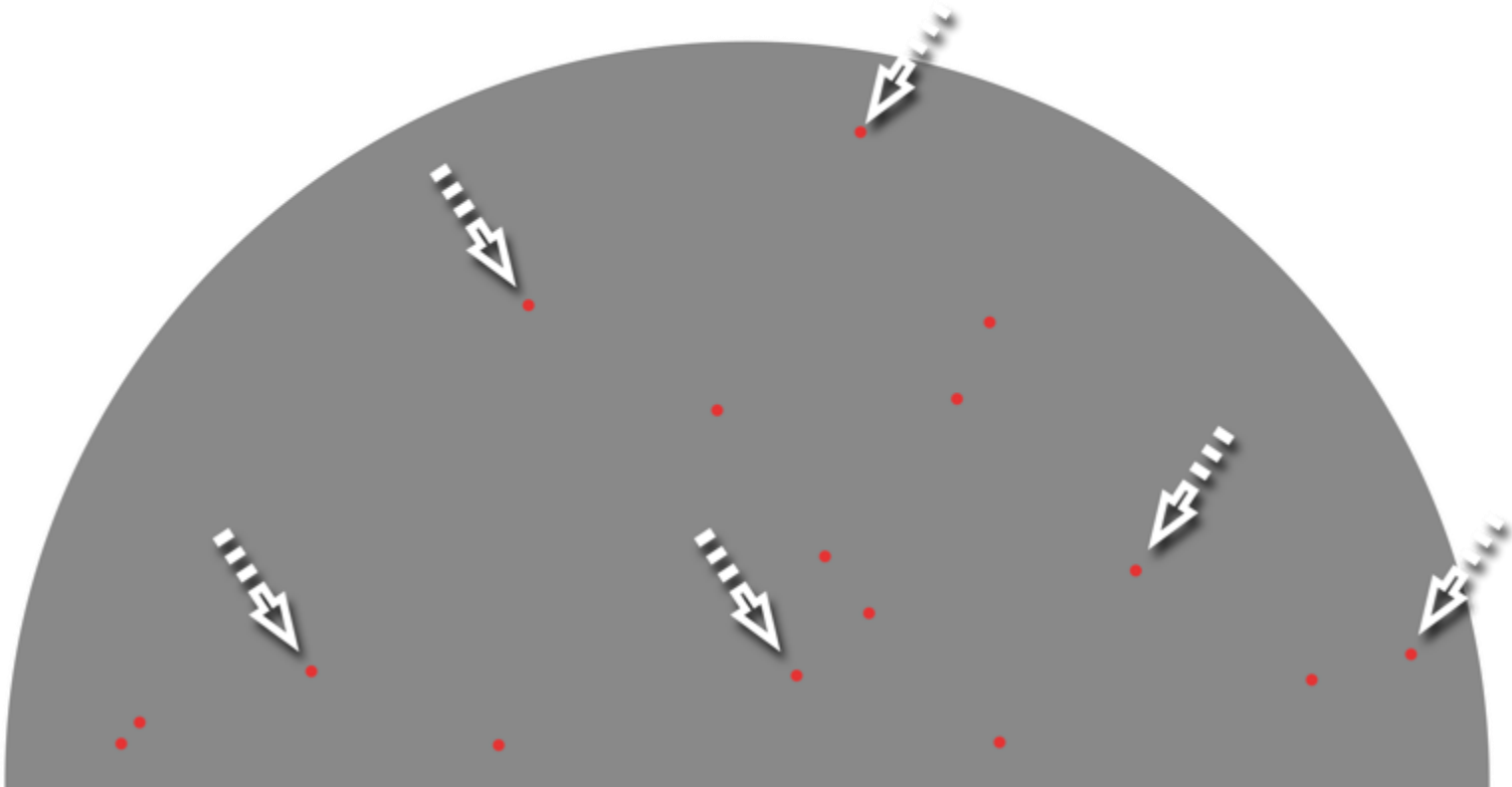


Let's explore the question of yield ...

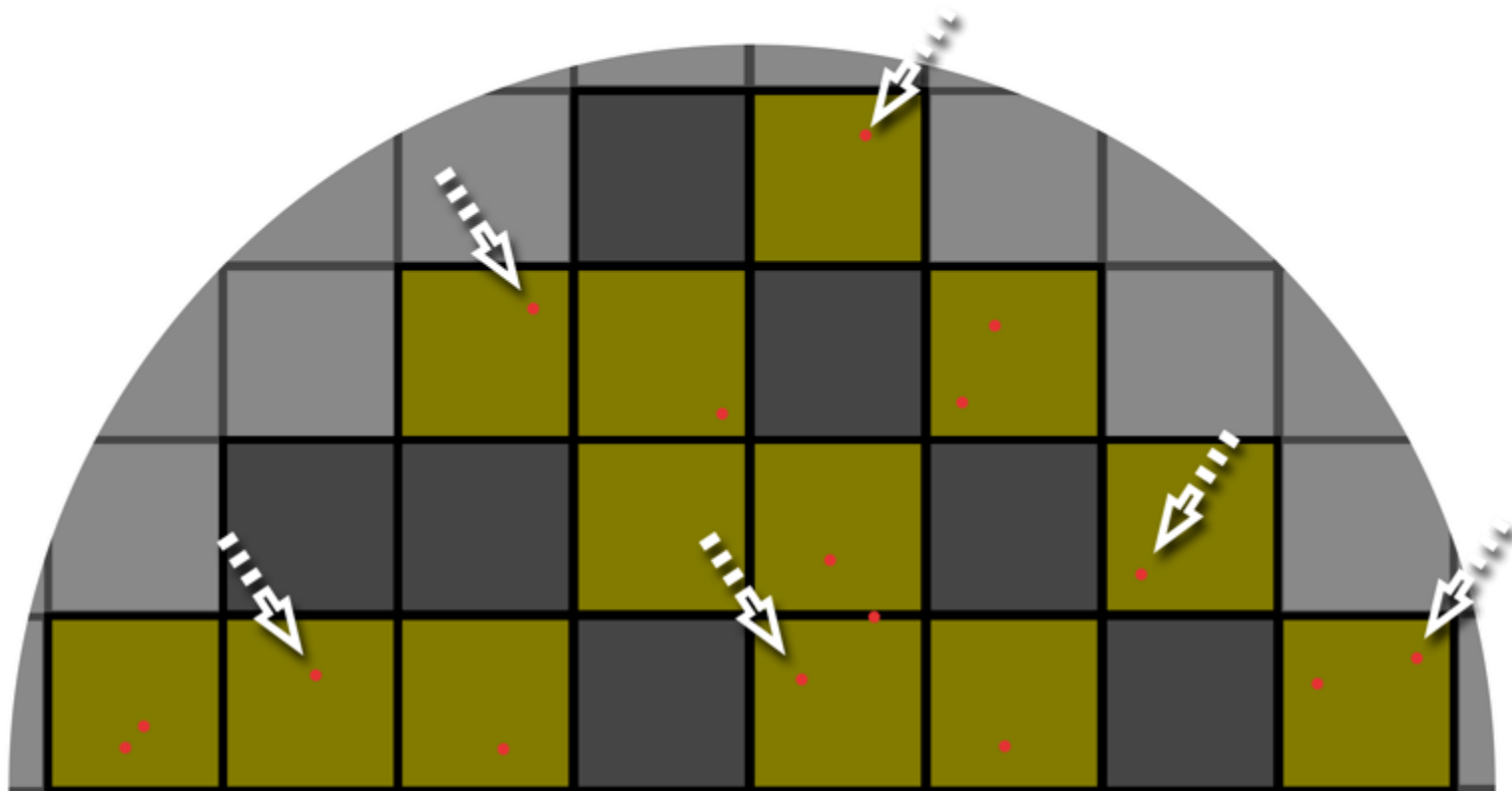


# The Silicon Wafer

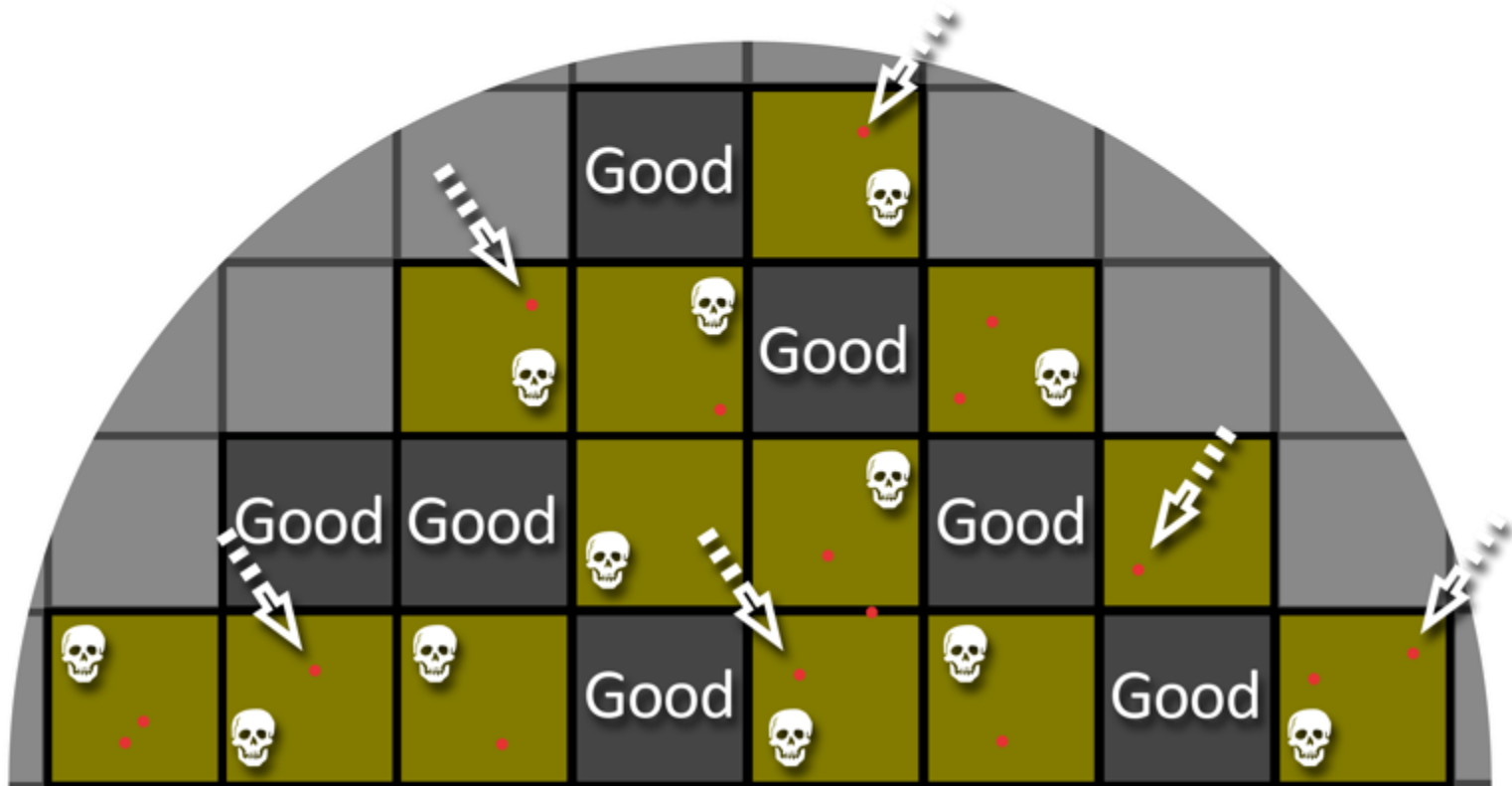
# Every Wafer Has Impurities

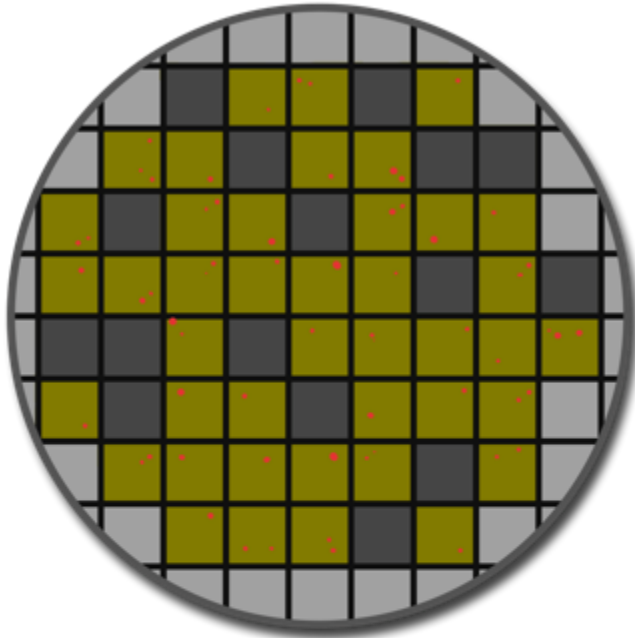


## Problem hits after masking ...



# Not all ASICs are good ...

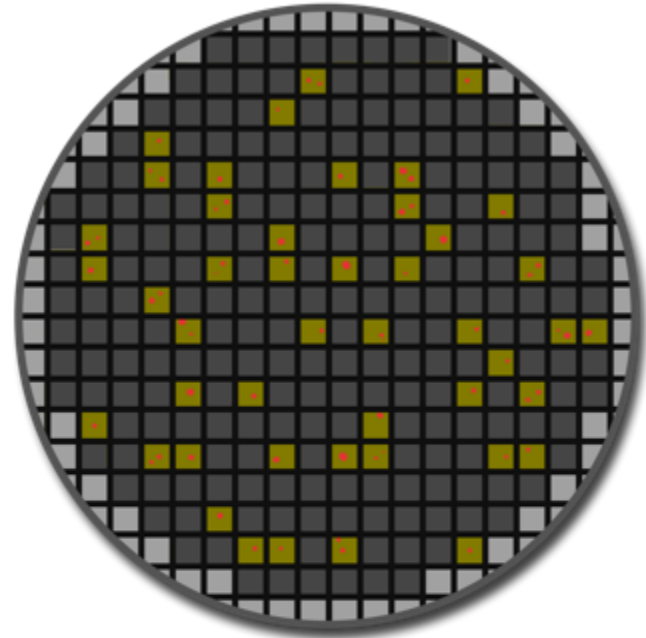




Die Size : 40mm x 40mm

Good: 16 | Bad : 42

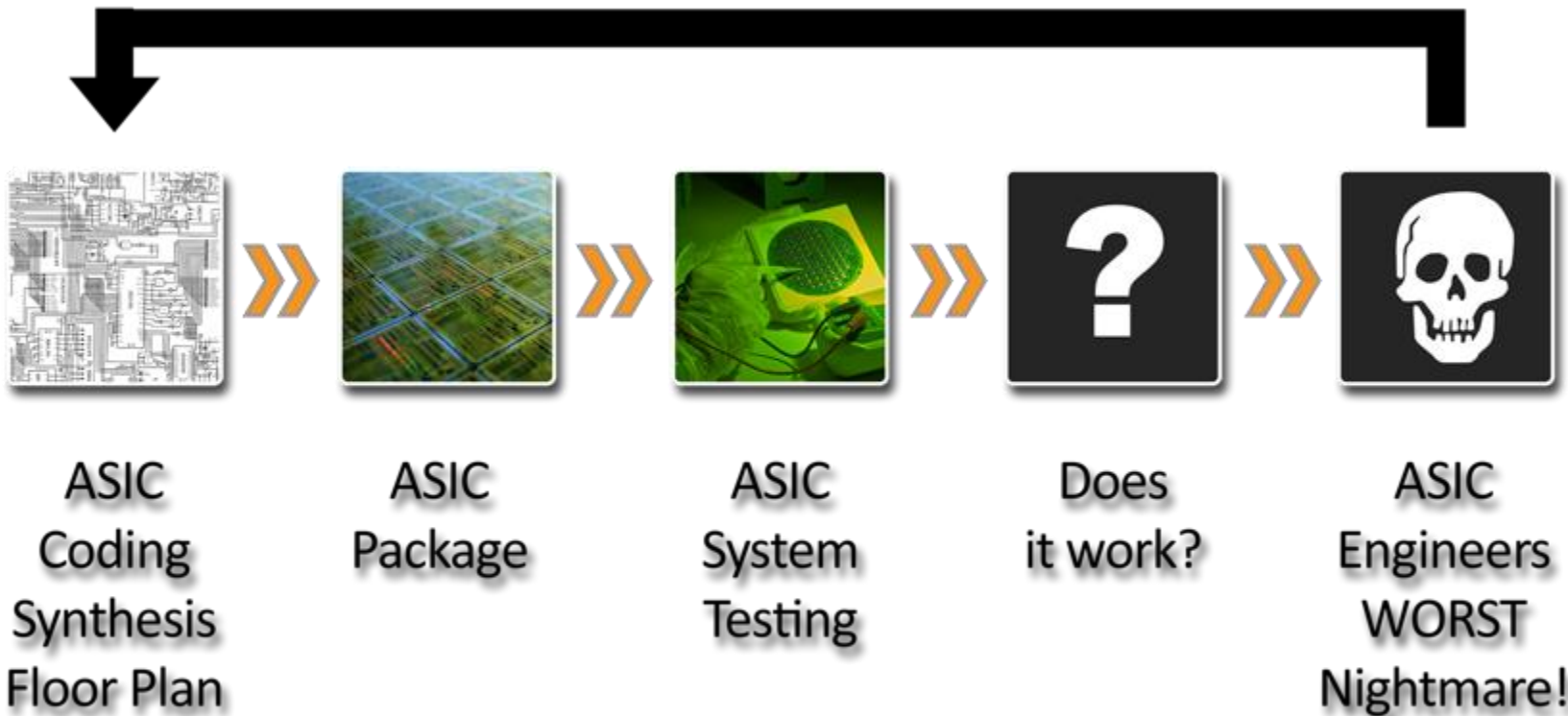
Yield : 27.6%



Die Size : 20mm x 20mm

Good: 212 | Bad: 46

Yield : 82.2%



ASIC Re-Spin (if needed)

# Agenda

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- How is an ASIC Developed?
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- UADP
- Summary





MARVELL



Custom  
VS  
Merchant



© 15-14713-01  
Doppler  
9BNX4C1  
P9F095K3-2  
1031 AOE EX  
TZ

# Why Merchant?



## Time to market opportunities

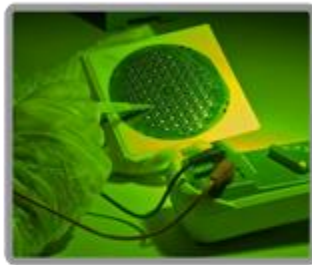
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Specifications  
meet customer  
requirements

Standard based  
capabilities

# Why does Cisco develop our own silicon?





# Five Reasons Why



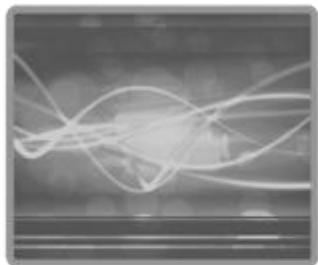


# Innovation

## Examples

New Functionality (CAPWAP, VxLAN, etc)  
Low Latency Switching  
Advanced QoS  
Security Enhancements  
Programmable Pipeline

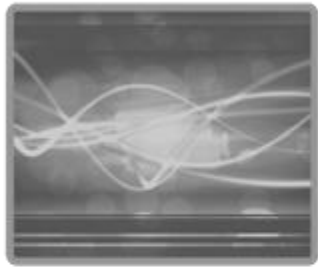
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# Optimisation

## Examples

Integrated Stacking Support  
Rapid Recirculation (Encapsulations)  
Advanced Functionality (VSS, StackPower)  
Visibility (Full NetFlow)  
Security (MACsec, SGTs)

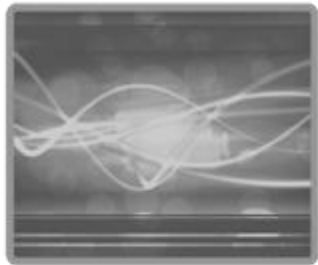


## Economies of Scale

Cisco total silicon business is  
several times the size of competitors

We deploy our ASICs into some  
of the largest run rate platforms  
in the industry

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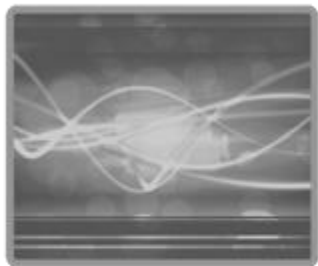


# Leading the Market

Examples

Wired / wireless integration (CAPWAP)  
Instant Access (VNtag)  
TrustSec (SGTs, SGACLs)  
SDN (OpenFlow, ONEpk)  
Advanced QoS and Traffic Visibility

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Delivering  
Business  
Value

Simplified Deployment Options  
Better Insight and Optimisation  
Increased Security  
Most Appropriate Scalability  
Flexibility and Investment Protection  
(programmability)

# Agenda

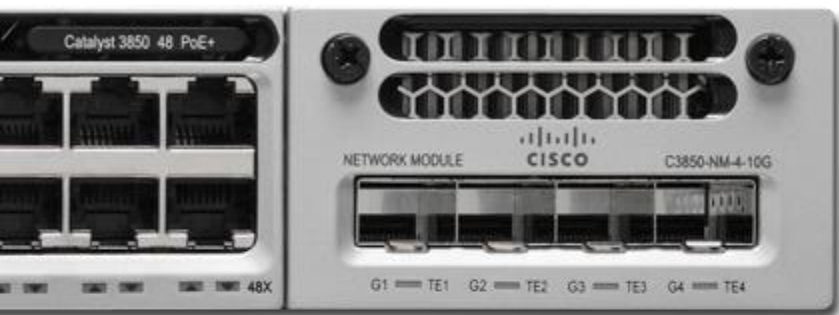
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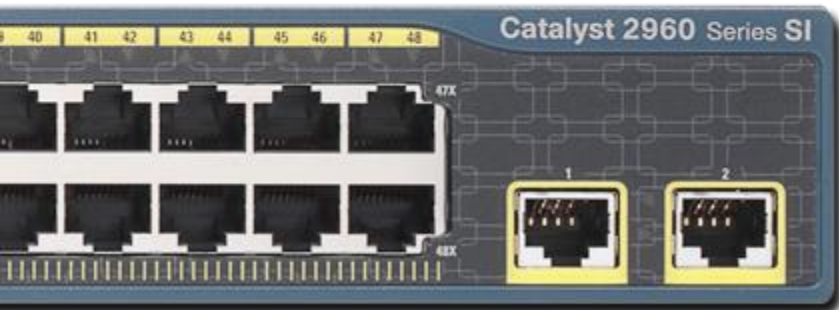
A long-exposure photograph of a city street at night. The foreground is filled with vibrant, multi-colored light trails from moving vehicles, creating a sense of motion. In the background, a modern cityscape is visible with illuminated buildings and a pedestrian bridge spanning the street. The overall scene is a blend of urban architecture and dynamic light patterns.

Cisco has a Long History of Enterprise  
Switching ASIC Innovation ...

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# Catalyst 29xx | 37XX | 38XX



Cat3750  
Cat2960  
180nm  
60M Transistors

## Catalyst 29xx

Cat2960S  
65nm

Cat2960X  
45nm



Cat3750E  
Cat3750X  
130nm  
210M Transistors

1.3B Transistors  
Cat3850 / 3650  
65nm



Cat3750G  
130nm

## Catalyst 3xxx

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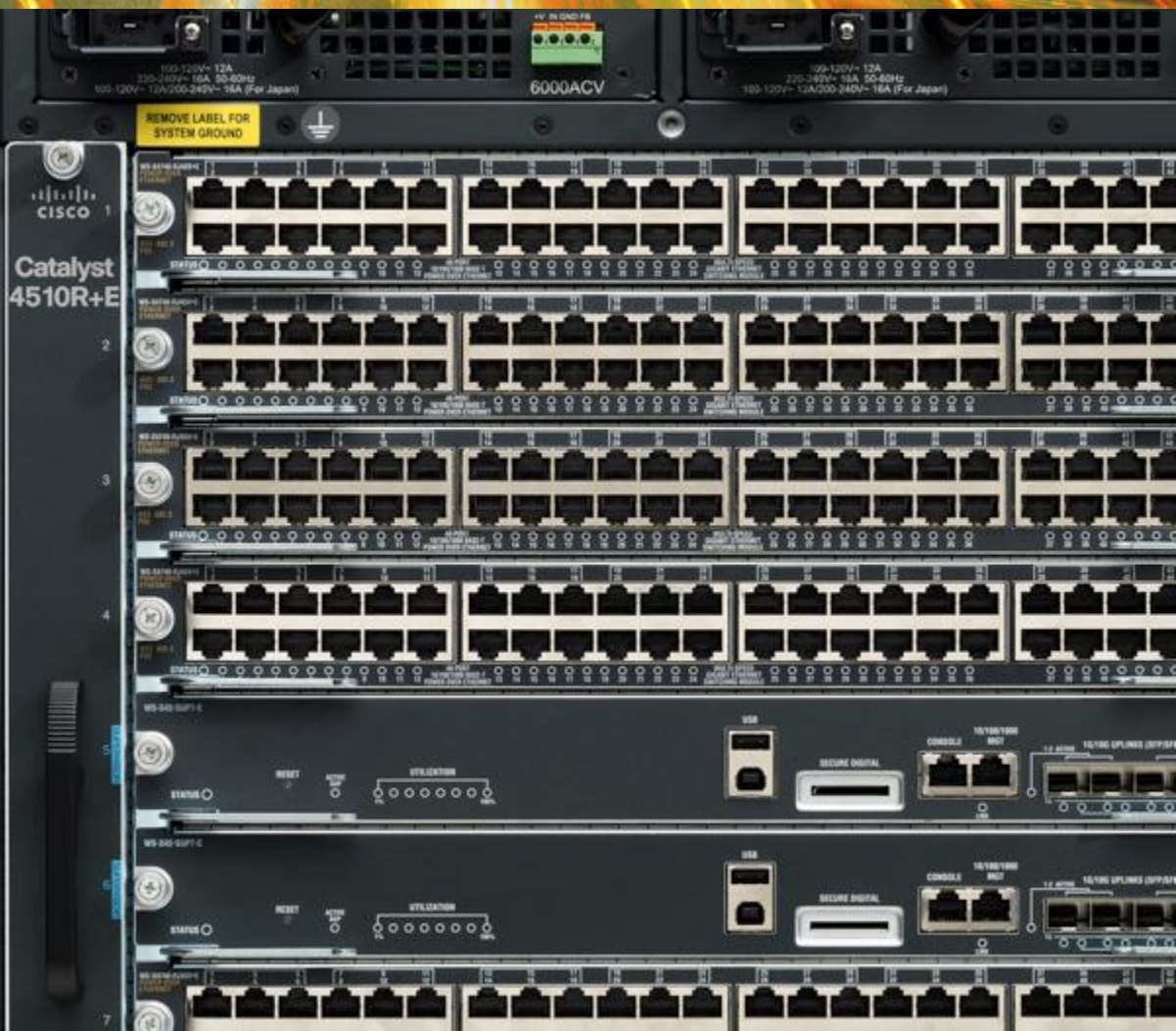
# Catalyst 29XX/3XXX

## ASIC Innovation

Support for StackWise stacking (32G stack), IPv4 Unicast and Multicast Routing, IPv6 Unicast Routing, Ingress and Egress Policing, Egress Shaping, SRR, WRED, 802.1Q and ISL support, Multiple SPAN sessions, RSPAN, Integrated packet buffer, External TCAM, uRPF, StackWise Plus (64G stack), SGT capability, IPv6 Multicast Routing (wide keys), Support for Jumbo Frame Routing (9216), Support for multiple First Hop Router Redundancy protocols at once, Hardware Merge TCAM, Integrated Hash Tables, Integrated associated data tables, Support for MadMax ASIC (Fabric with 4 stack ports), Support for Local Switching, FlexStack support, Low power -> Fanless possible, MACSec, ERSPAN, COPP ...



# Catalyst 4500



**K1**  
Sup1  
2000



**K2**  
Sup3  
2002



**K10**  
Sup7  
2010  
90nm  
1.2B Transistors



**K5**  
Sup6E  
2007  
90nm  
600M Transistors

Catalyst  
4000/4500  
ASIC Innovation

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# Catalyst 4000/4500

## ASIC Innovation

High-performance centralised switching – 492 Gbps L2 / L3 capacity, IPv4 and IPv6 forwarding in hardware, up to 250 Mpps Multicast, up to 60Gbps Recirculation bandwidth, 256K routes (128K IPv6) and 48K adjacencies, ECMP routing, Unicast RPF (strict and loose), VRF-lite (64 VRFs), EVN support, 64K input and 64K output ACEs, 8 bidirectional SPAN sessions, NetFlow (up to 128K flows), Advanced Congestion Avoidance: Dynamic Buffer Limiting (DBL), Smooth Round Robin (SRR) with sharing and shaping per queue, Granular per-port per-VLAN policies, IP Source Guard, 64 CPU queues with CoPP, large (32MB) high performance shared packet buffer, PVLAN support for promiscuous and isolated trunks, 1:1 & 1:N VLAN Translation, Packet & byte counters per adjacency, Policy-based Routing ...





# Catalyst 6500 6800





Catalyst 5000 / 5500 / 6000 / 6500 / 6800  
Nexus 7000

# Catalyst 5000/6500

## ASIC Innovation

IPv6 Unicast + Multicast in Hardware, RSPAN, ERSPAN, GOLD, OBFL, ACL Merge Optimisation, Netflow, MPLS in Hardware, IGMPv3, EoMPLS, VPLS, A-VPLS, NAT, PAT, RBACL, Egress Multicast Replication, Full and Sampled Netflow, Ingress/Egress Netflow, IPv4 Tunnelling, GRE, IPv6 Tunnelling, 6to4 Tunnelling, ISATAP Tunnelling, Recirculation, Bridge Domains, Static MAC match conditions, Virtual Switch Link, Bi-Directional PIM, Control Plane Policers, HW Rate Limiters, Ingress/Egress Aggregate Policers, Microflow Policers, VSS support, Strict and Loose RPF Check, HW PIM Register Encap/Decap, MPLS QoS, Ingress/Egress DSCP Mutation, QPPB, SGT, 3 Colour Policing, MLD Snooping, RBH for Etherchannel Mapping, Port Security, Optimised IP Multicast Flooding, 16 Way ECMP ...

EARL1  
(1995)



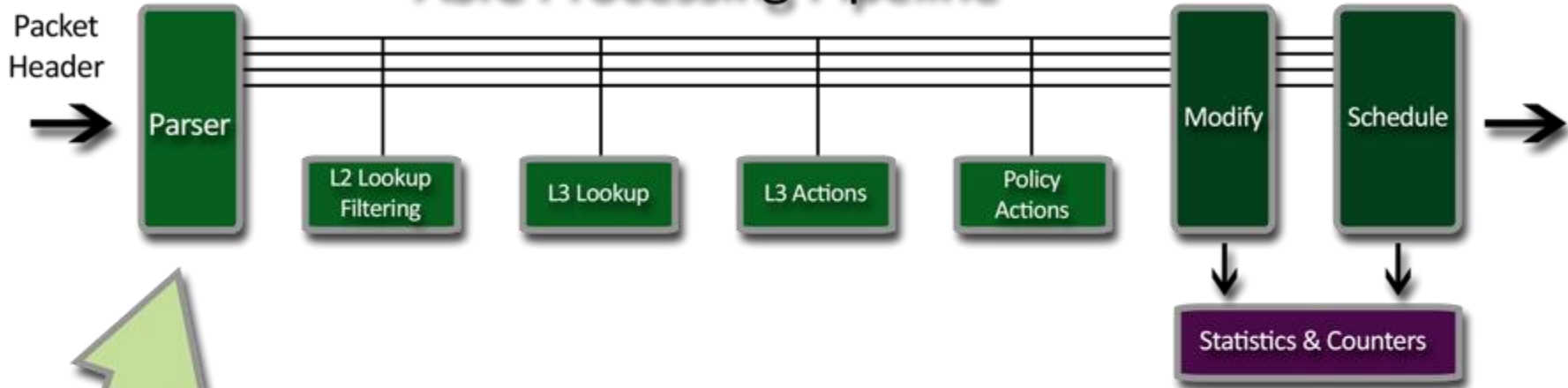
EARL8  
(2011)

# Agenda

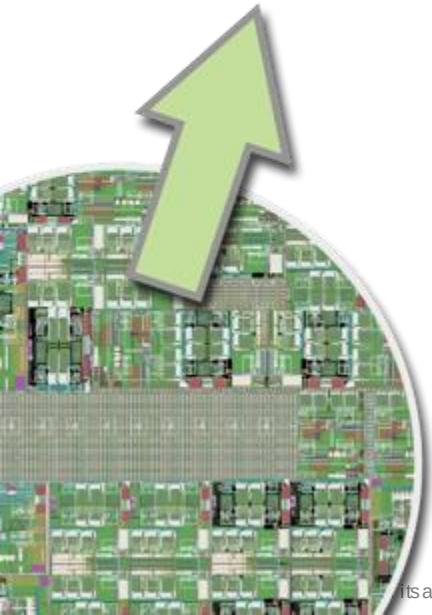
- Why ASICs?
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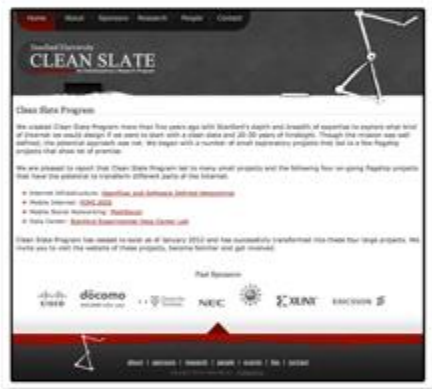


## ASIC Processing Pipeline



Traditionally the pipeline is  
**FIXED**





## Clean Slate SDN Ground Zero



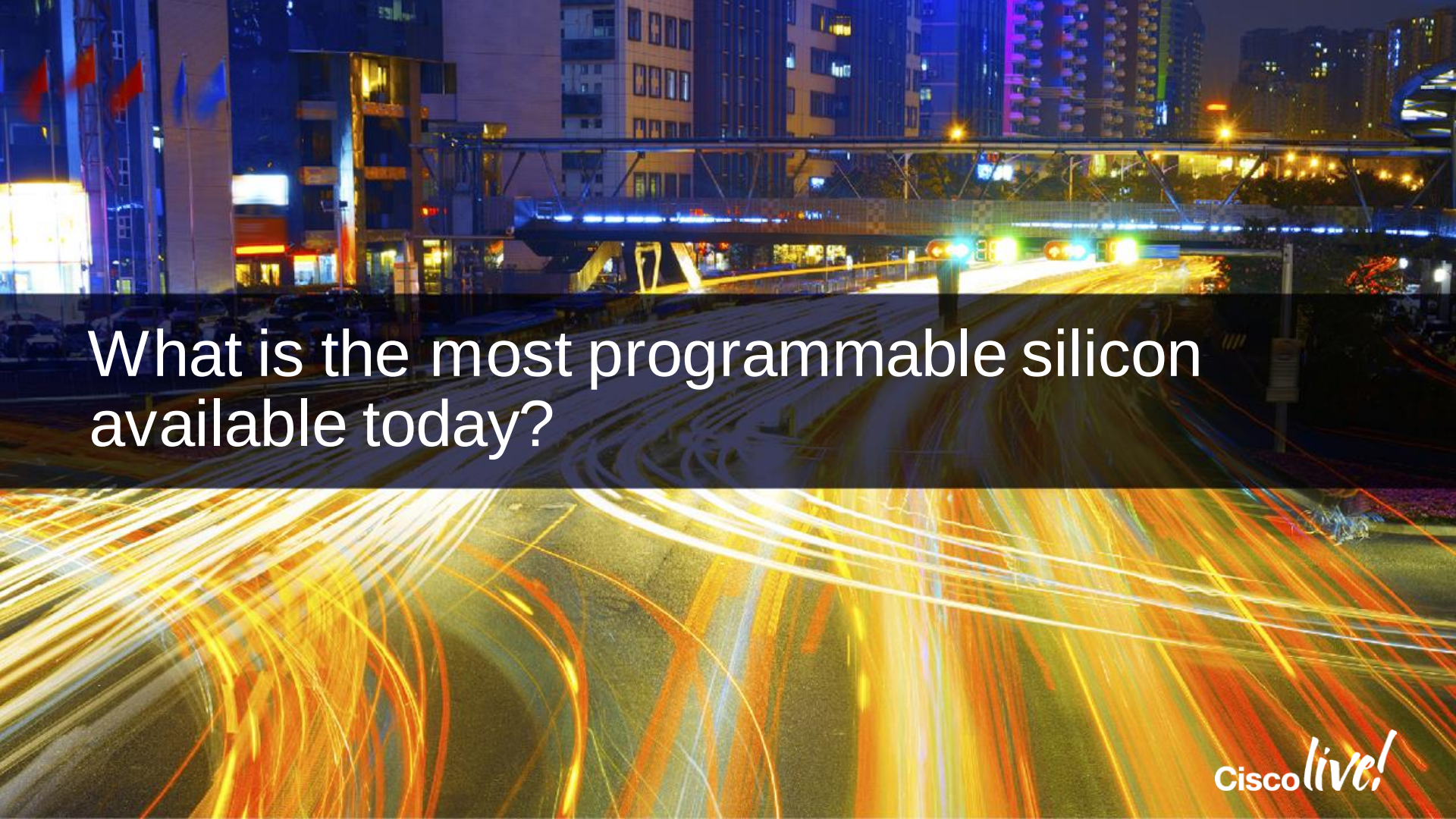
OPENFLOW

OVERLAYS

ASICs

ORCHESTRATION

AND MORE

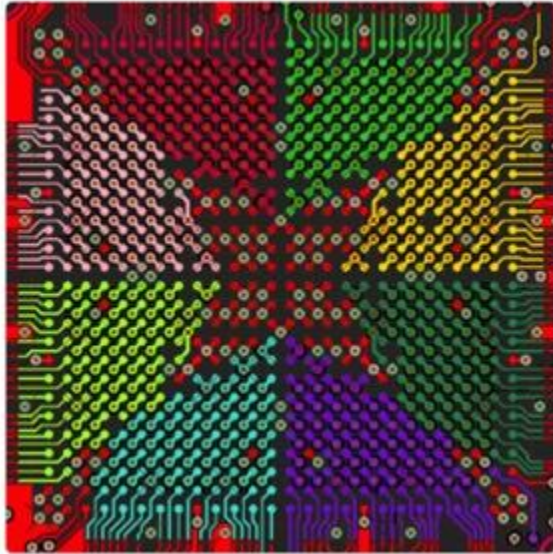


What is the most programmable silicon available today?



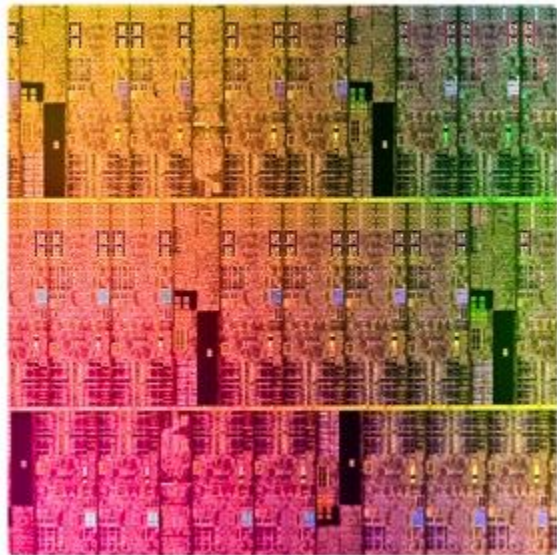
The General  
Purpose CPU...

Very Flexible  
**BUT SLOW...**



# Field Programmable Gate Array (FPGA)

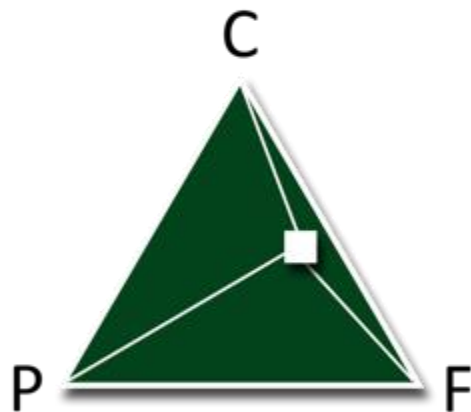
Flexible  
And Faster  
But Costlier...



# The Network ASIC ...

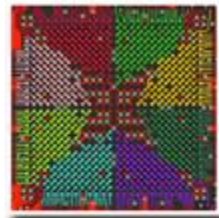
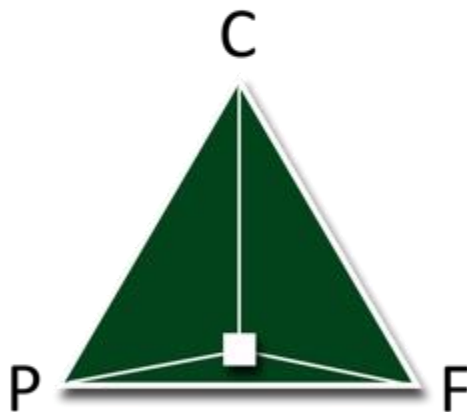
## Very Fast BUT FIXED...

## Traditional CPU



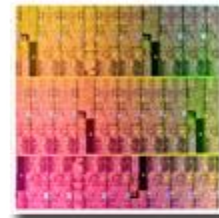
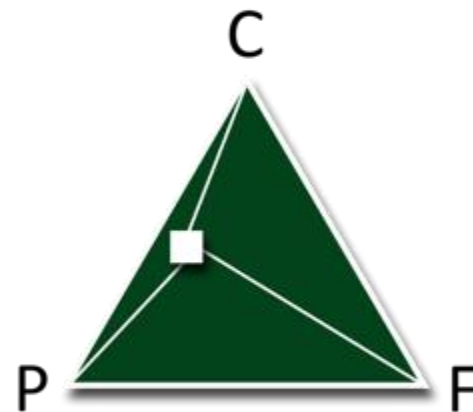
COST ~  
PERFORMANCE  
FLEXIBILITY ✓

## FPGA



COST ✖  
PERFORMANCE ✓  
FLEXIBILITY ✓

## Network ASIC

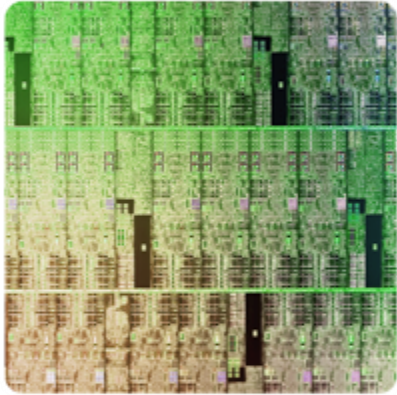
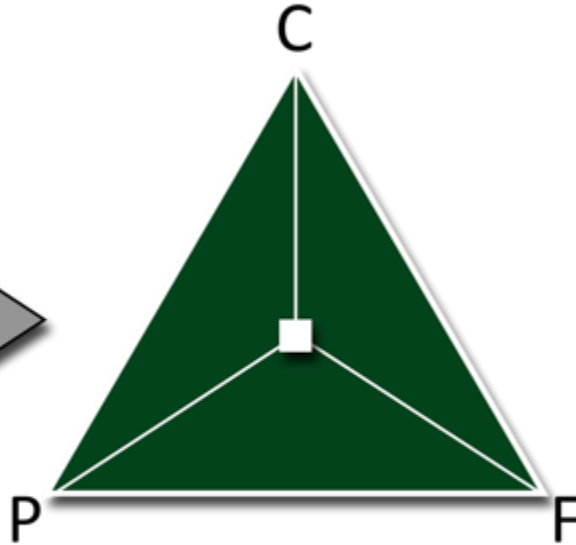


COST ✓  
PERFORMANCE ✓  
FLEXIBILITY ✖



So where can programmable ASICs help us?

# Programmable ASIC



COST ✓

PERFORMANCE ✓

FLEXIBILITY ✓

# Programmability introduces flexible pipelines...



**ASIC  
Engineer**

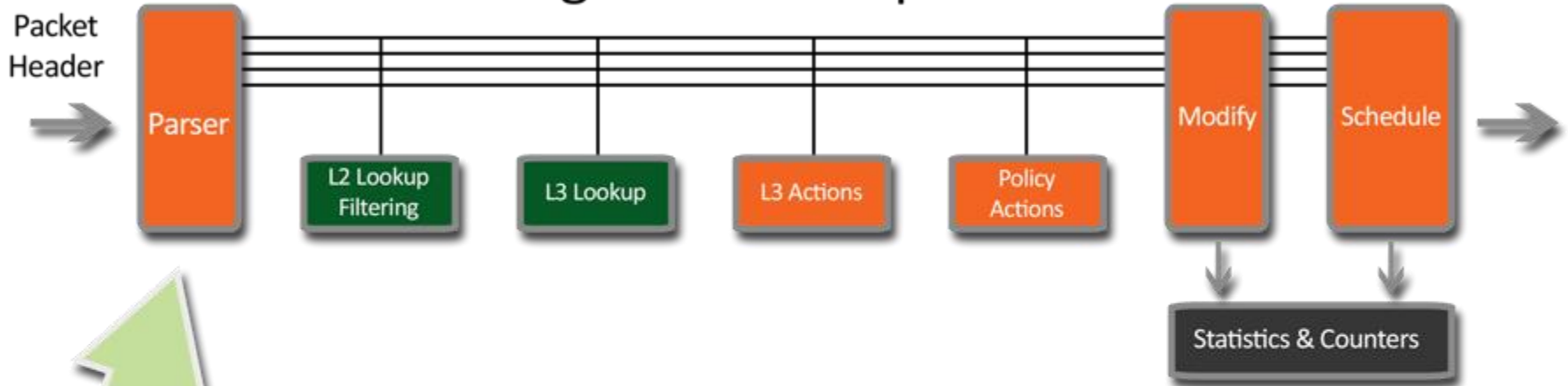


**Microcode  
Update**

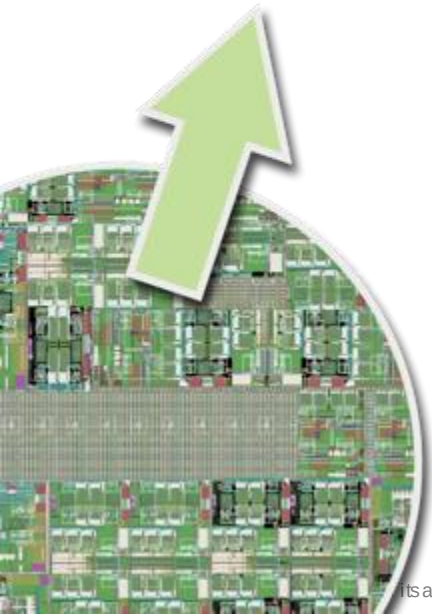


**New ASIC  
Functionality**

# ASIC Programmable Pipeline



Modify processing behaviour  
without incurring re-spin



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A long-exposure photograph of a city street at night. The foreground is filled with vibrant, multi-colored light trails from moving vehicles, creating a sense of motion and energy. In the background, modern city buildings are illuminated with various lights, and a pedestrian bridge spans the street. The overall scene is a dynamic urban environment.

# Programmable Routing Silicon – Quantum Flow Processor (QFP)



Performance  
Programmability  
Flexibility



# Evolution of Routing



## QUANTUM FLOW PROCESSOR (QFP)



High Performance



Programmable



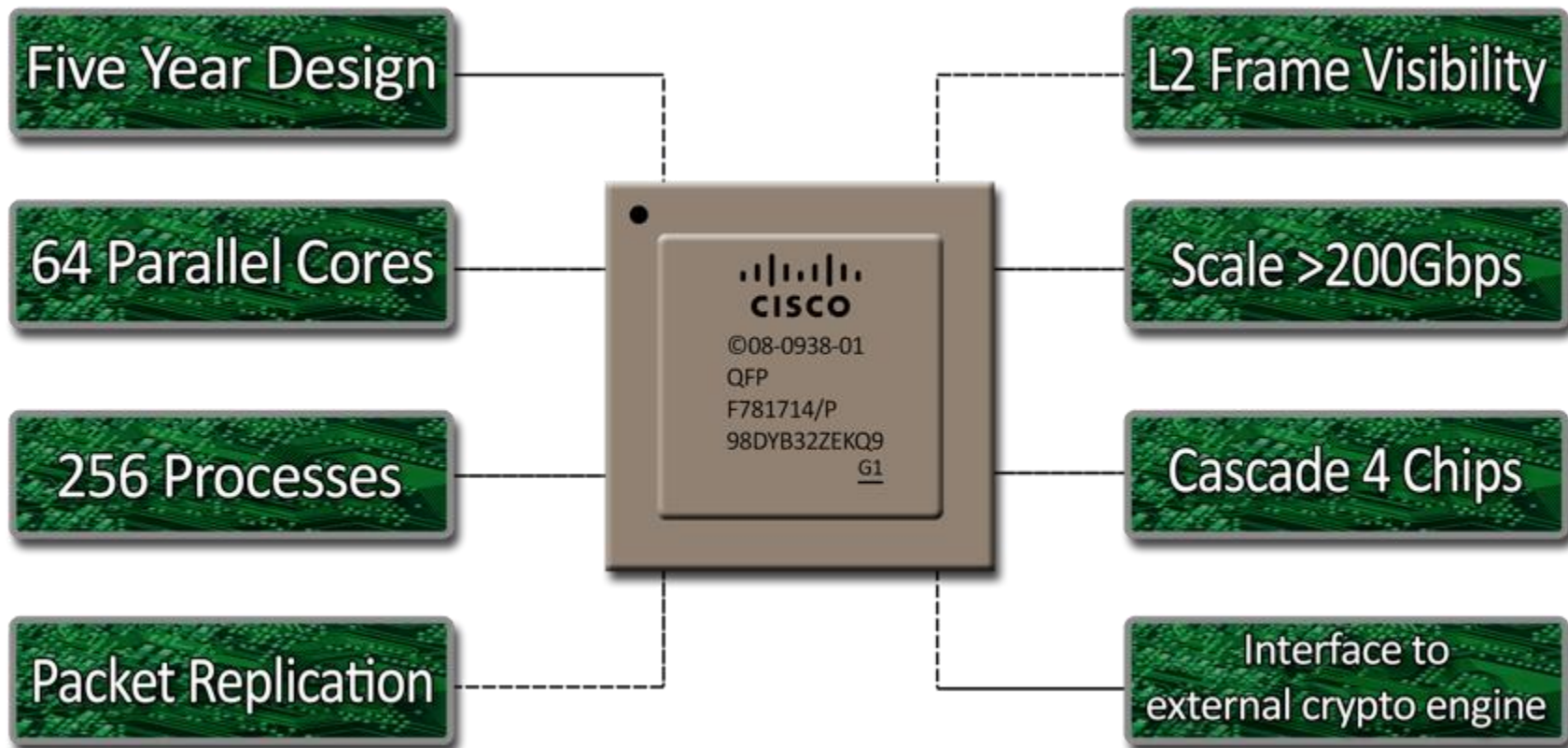
Feature Rich



Price/Performance



Longevity/Flexibility



100% Developed Cisco Networking Silicon

Cisco *live!*

QFP-1  
Multi Core  
Packet Processor



Traffic Manager  
and Interface Chip



QFP-2



...



# QFP Development History

Cisco *live!*

QFP-1  
Multi Core  
Packet Processor



Traffic Manager  
and Interface Chip



QFP-2



...



# QFP Development History

Cisco *live!*

# QFP-1

Multi Core  
Packet Processor

Traffic Manager  
and Interface Chip

QFP-2

...

1.2 GHz / 400 MHz

40 custom  
multi-threaded CPUs

90nm, 8-layers metal

382 mm<sup>2</sup>

307 million transistors

1019 I/O, including  
800 MHz DDR



Traffic Manager  
and Interface Chip



QFP-2



...



# QFP-1

Multi Core  
Packet Processor

|                                           | Cisco QFP      | Sun<br>UltraSparc T2 | Intel Core 2<br>Mobile U7600 |
|-------------------------------------------|----------------|----------------------|------------------------------|
| Total #<br>Processes<br>(Cores x Threads) | 160            | 64                   | 2                            |
| Power per<br>Process                      | 0.51w          | 1.01W                | 5W                           |
| Scalable traffic<br>management            | 128K<br>Queues | None                 | None                         |

# QFP-1

Multi Core  
Packet Processor



# QFP-2

...



## Traffic Manager & Interface Chip

400 MHz

Buffering, 128K queues  
Hardware HQF  
scheduling

90nm, 8-layers metal

332 mm<sup>2</sup>

522 million transistors

1318 I/O, including  
800 MHz DDR

# QFP-1

Multi Core  
Packet Processor



## Traffic Manager and Interface Chip



...



# QFP-2

1.2 GHz / 400 MHz

64 custom  
multi-threaded CPUs

Up to 1500 MHz  
Buffering,  
116K queues

Hardware HQF  
scheduling

40nm, 10-layers metal  
324 sq mm  
1.8 Billion transistors

1480 I/O, including  
800 MHz DDR

QFP-1  
Multi Core  
Packet Processor



Traffic Manager  
and Interface Chip

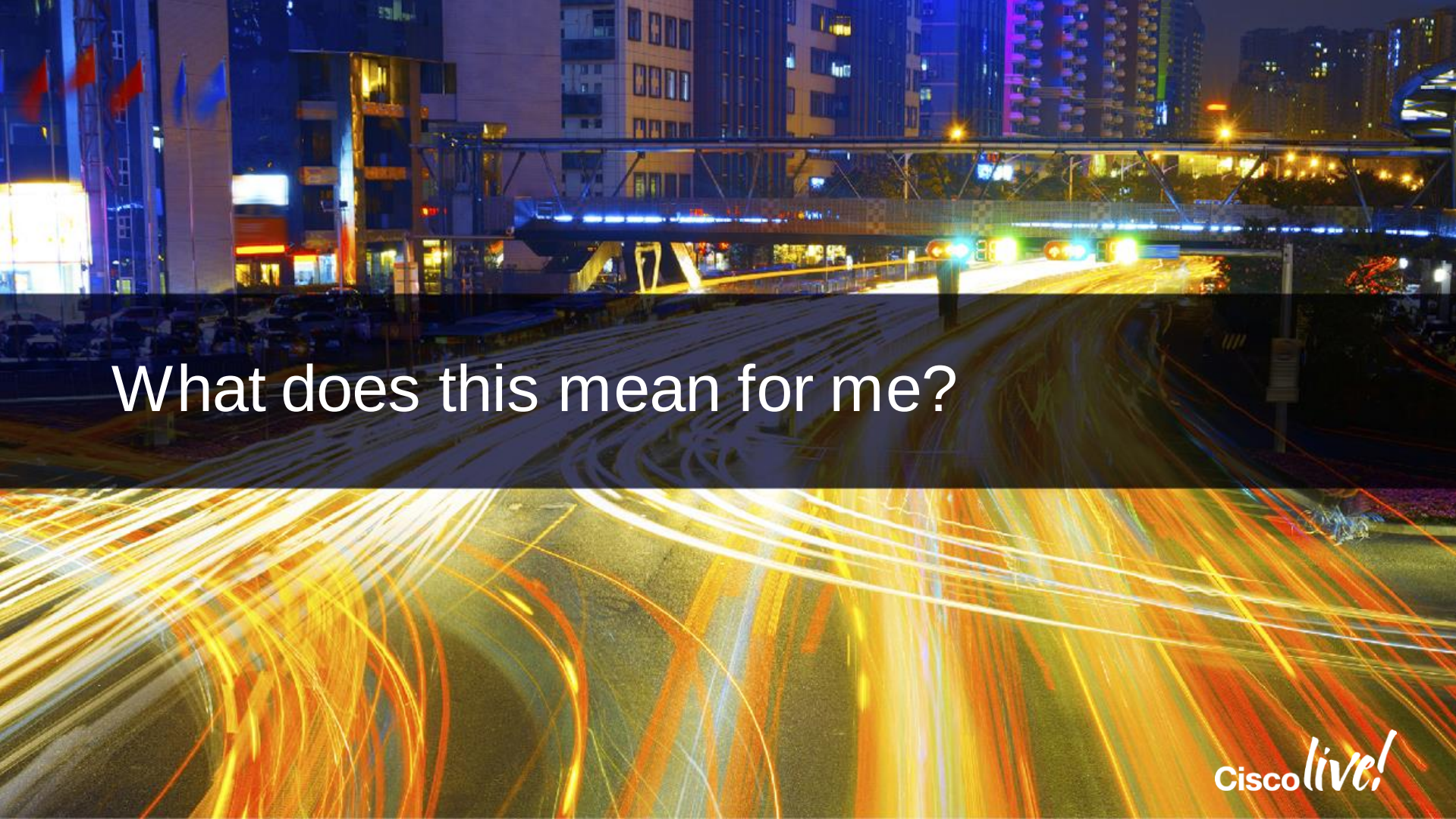


QFP-2



More  
to  
Come





What does this mean for me?



# QFP Programmable Hardware

equals

FLEXIBILITY  
PERFORMANCE

# QFP-1

Multi Core  
Packet Processor



# QFP-2



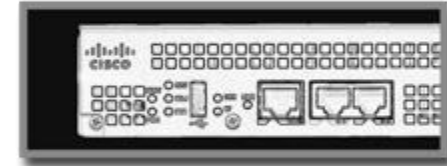
...



ASR 1001. 1002  
1002-F, ESP-5, ESP-10  
ESP-20, ESP-40,  
ASR-9000 SIP



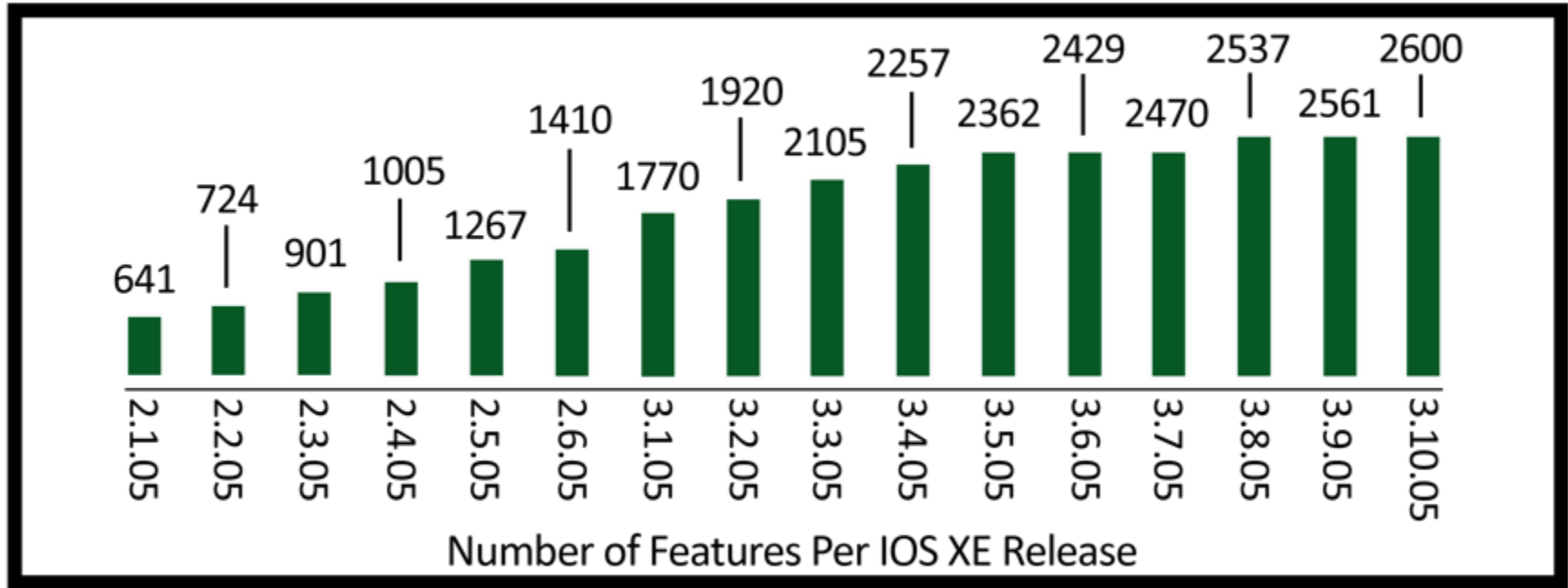
ASR 1002-X  
ESP-100, ESP-200



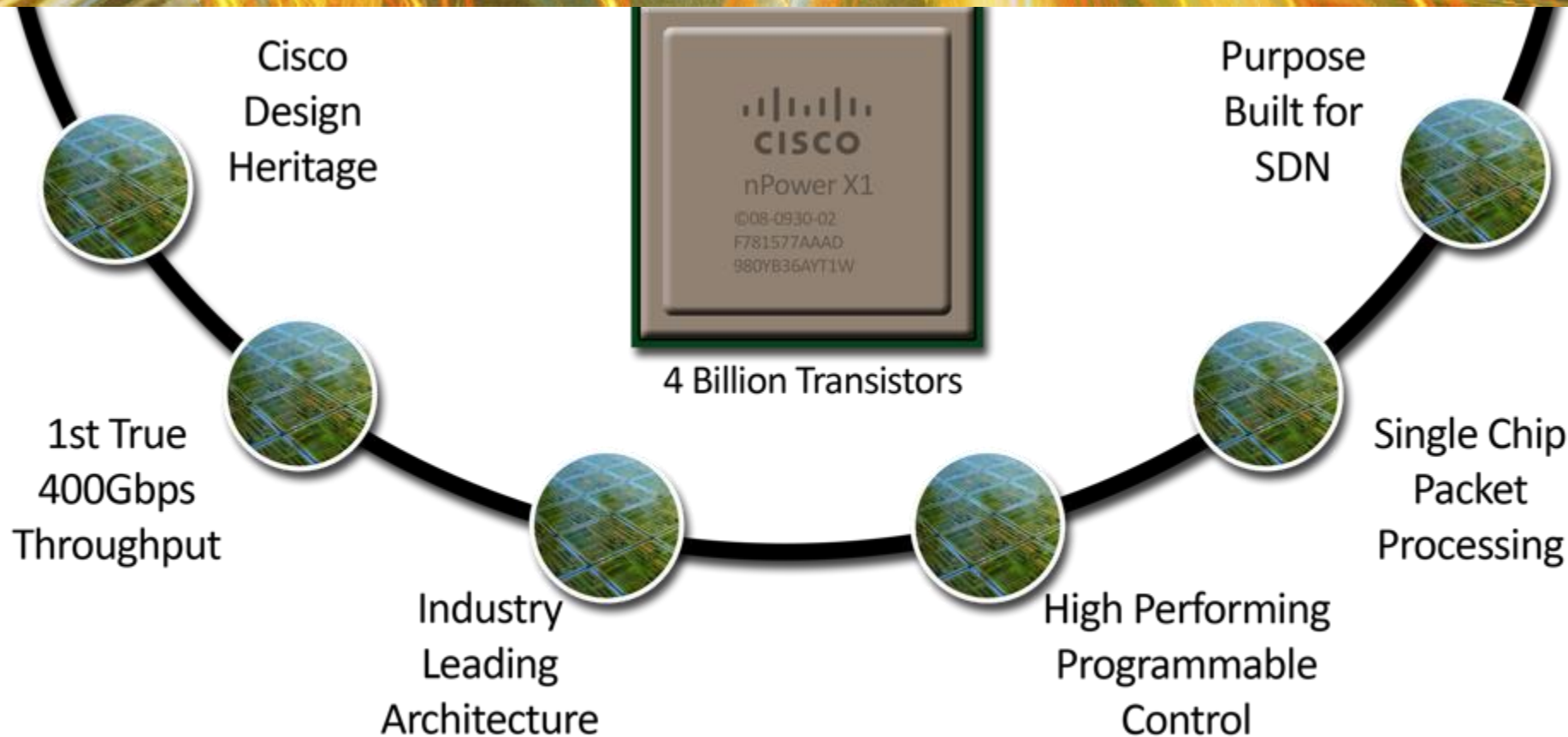
More to come

# QFP Platforms

# QFP Feature Velocity



Over 2600 features



# Next-Gen Network Processor - nPower X1

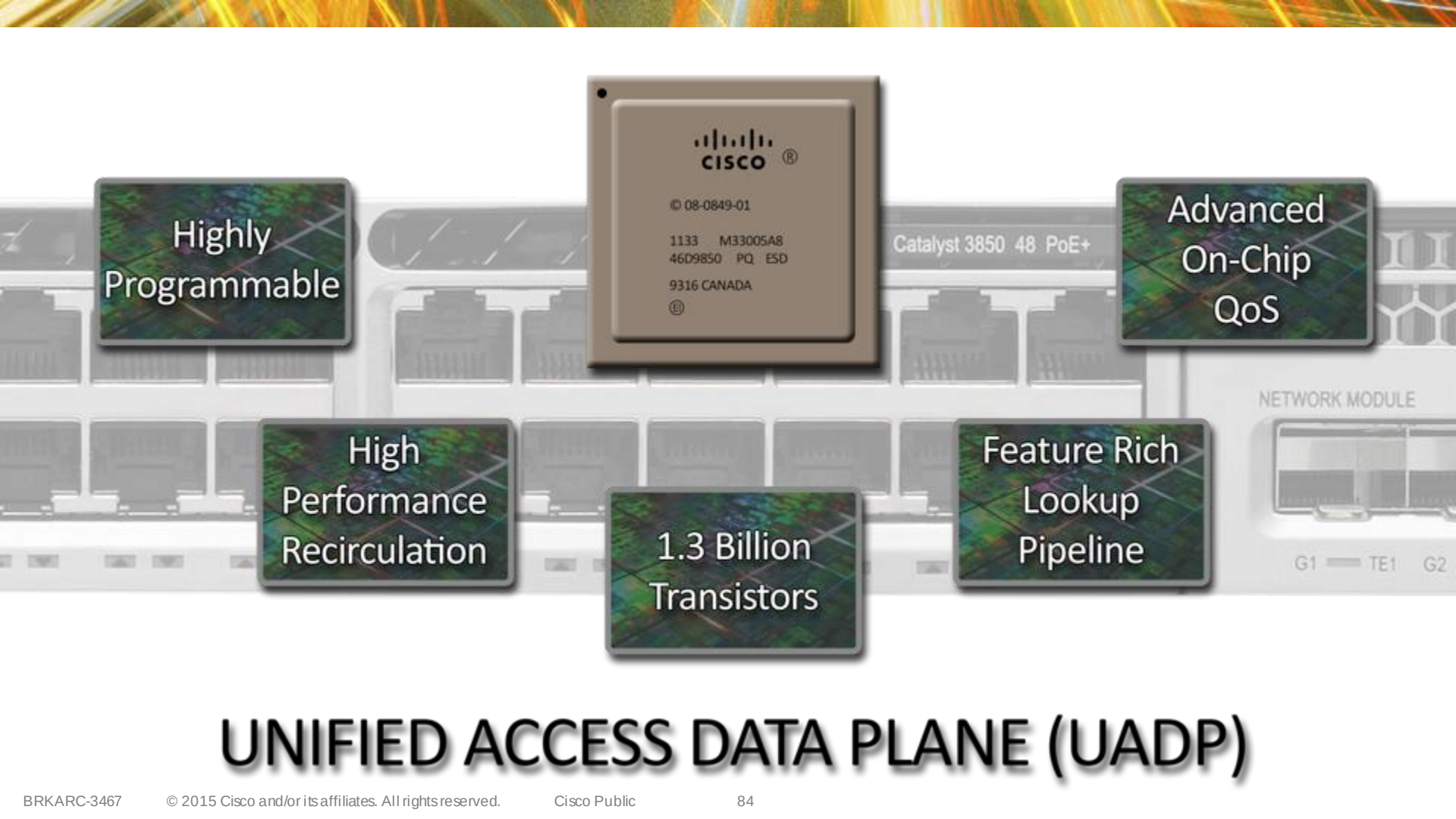
# Agenda

- Why ASICs?
- How is an ASIC Developed?
- Merchant vs. Custom
- Cisco ASIC History
- The Move to Programmability
- QFP
- UADP
- Summary



A long-exposure photograph of a city street at night. The background shows tall buildings with lit windows and a pedestrian bridge. The foreground is dominated by vibrant, multi-colored light trails from moving vehicles, creating a sense of motion and energy. The text is overlaid on a dark horizontal band across the middle of the image.

# Programmable Switching Silicon – Unified Access Data Plane (UADP)

A Cisco Catalyst 3850 48 PoE+ network module is shown against a background of a server rack. The module is a brown square with a Cisco logo and technical specifications. Six callout boxes with a green and black grid pattern point to various features of the module.

Highly  
Programmable

© 08-0849-01

1133 M33005A8  
46D9850 PQ ESD

9316 CANADA



Advanced  
On-Chip  
QoS

High  
Performance  
Recirculation

1.3 Billion  
Transistors

Feature Rich  
Lookup  
Pipeline

NETWORK MODULE

G1 TE1 G2

# UNIFIED ACCESS DATA PLANE (UADP)

1

2

3

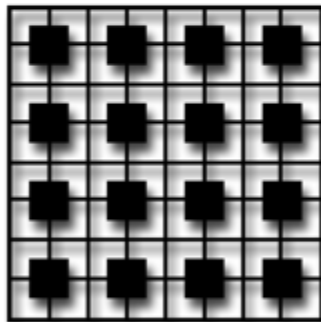
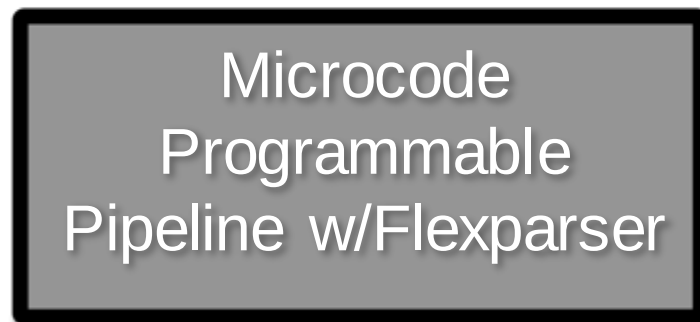
4

5

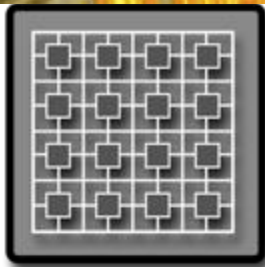
## 5 Key Capabilities



# UNIFIED ACCESS DATA PLANE (UADP)



# UNIFIED ACCESS DATA PLANE (UADP)



2

3

4

5

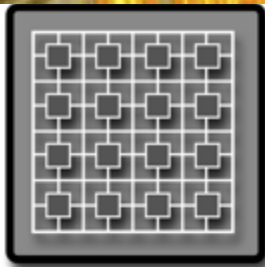
Stack Master

Stack Member

Stack Member

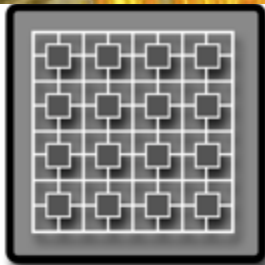
240G  
Stacking Interface  
integrated into ASIC

## UNIFIED ACCESS DATA PLANE (UADP)



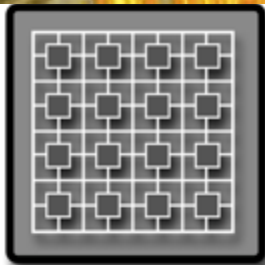
On Chip Micro Engines  
Fragmentation /  
Reassembly, Encryption /  
Decryption (AES-128, CBC)

# UNIFIED ACCESS DATA PLANE (UADP)



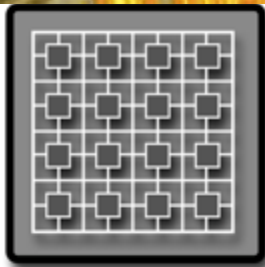
High-Performance  
Recirculation Path  
(less than 1usec  
Recirculation Latency)

# UNIFIED ACCESS DATA PLANE (UADP)



Integrated On Chip  
Netflow  
24K Entries

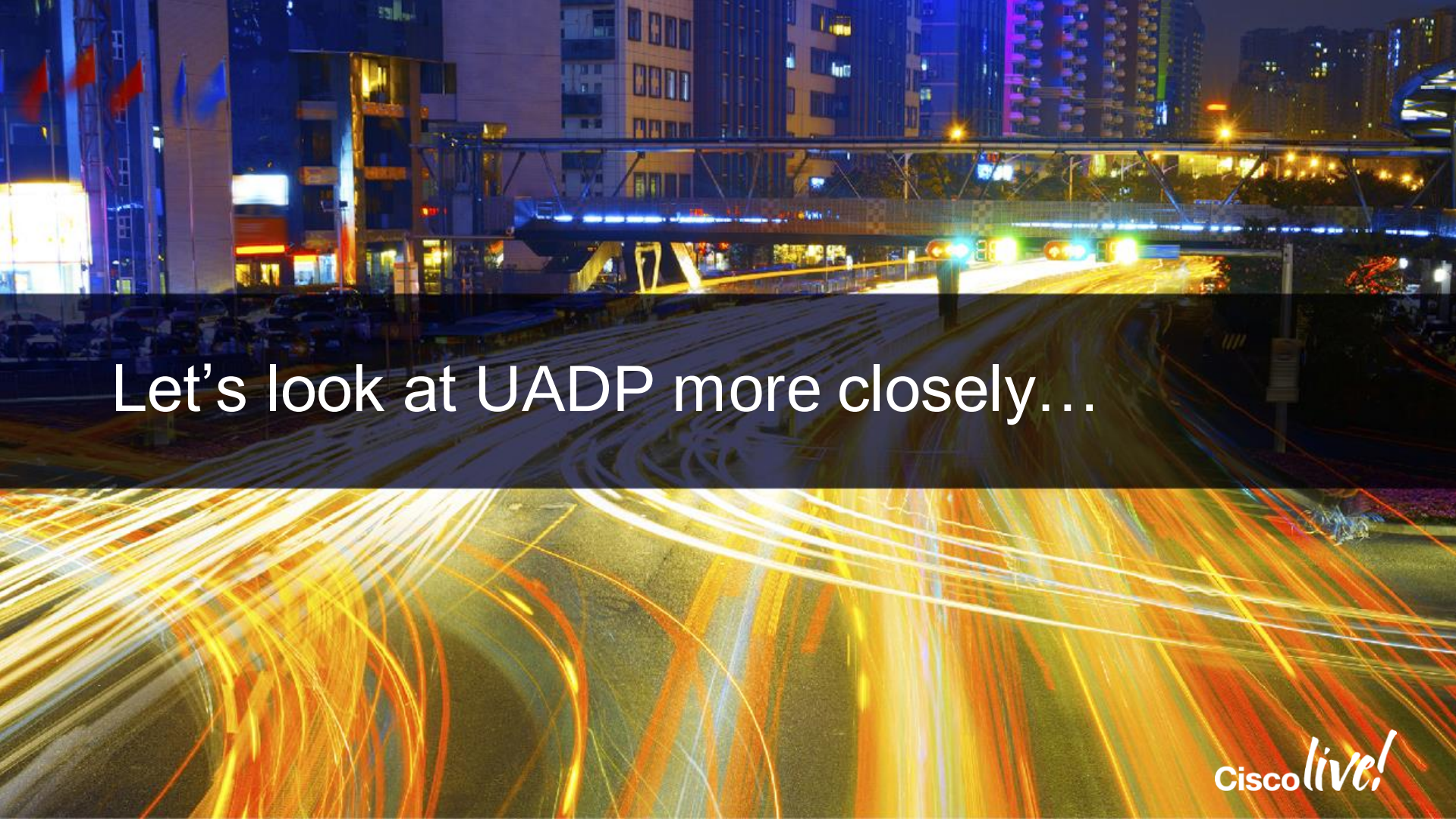
# UNIFIED ACCESS DATA PLANE (UADP)



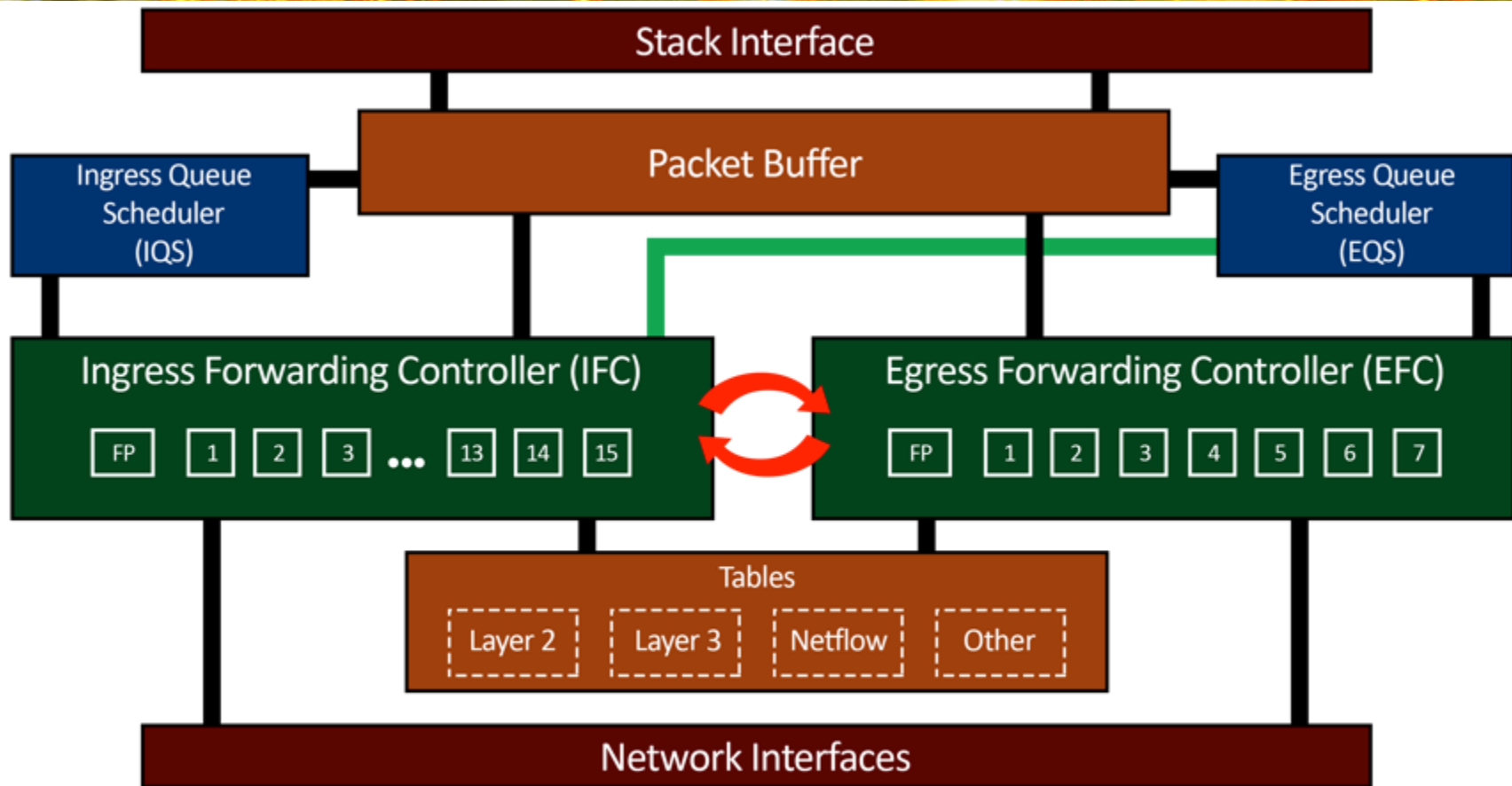
Stack spatial reuse | Local switching | Jumbo frames | 8 egress queues per port |  
Dynamic fair buffer sharing | Active queue management | WRED |  
Approximate Fair Drop | Per Flow counters | Control Plane Protection |  
SRR scheduling | Microflow 1R2C policers | Aggregate 2R3C policers |  
Policer chaining | Class-based flow control | Packet parser | Unicast RPF |  
Private VLANs | PBR | IGMP / MLD snooping | SGT support | Role-based ACLs |  
Policy-based ACLs | Client-based or Group-based ACLs | L2 / L3 tunnel support |  
CAPWAP | DTLS | sRTP | Embedded logic analyser |  
SPAN, RSPAN, ERSPAN, Flow SPAN ...

Features noted are  
hardware capable  
with UADP, but are  
not yet necessarily  
productised

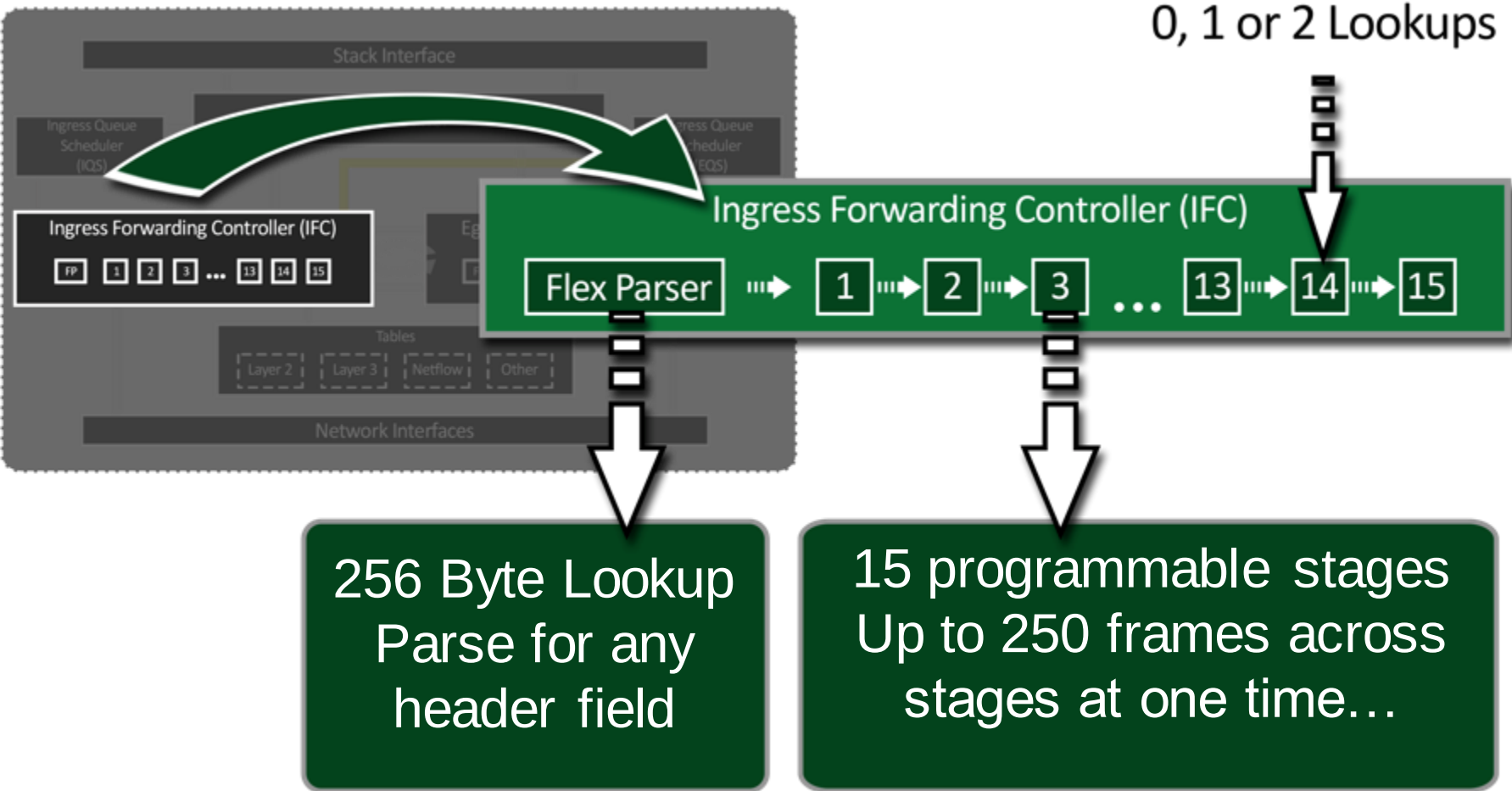
# UNIFIED ACCESS DATA PLANE (UADP)

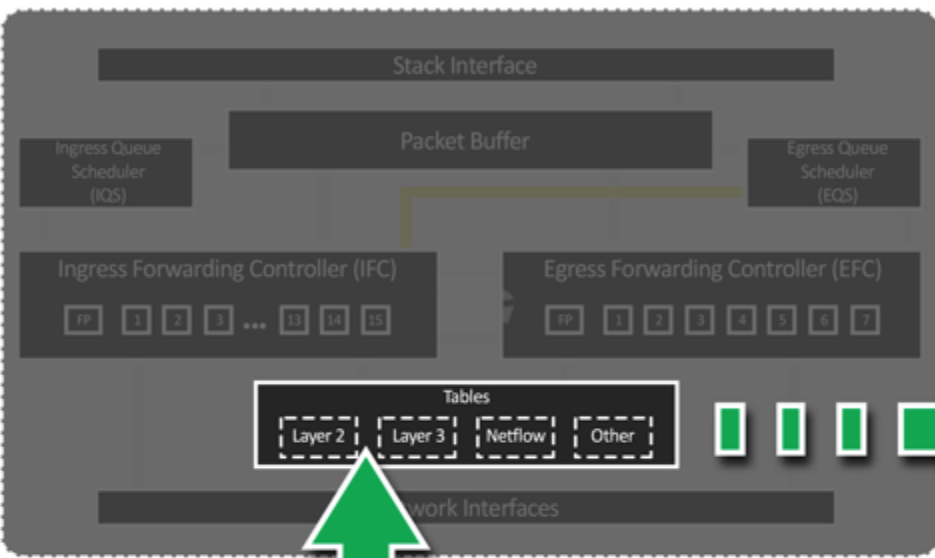
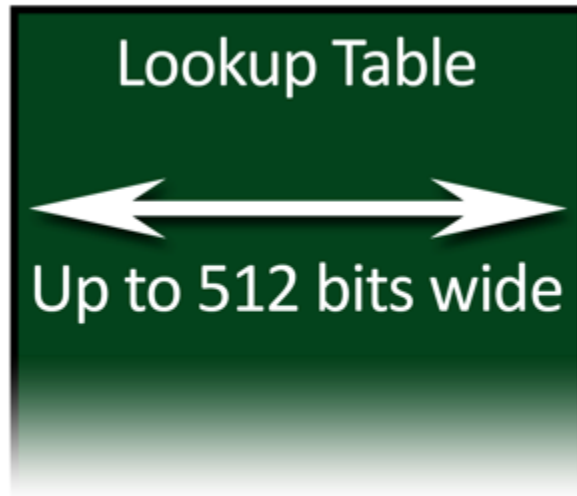


Let's look at UADP more closely...



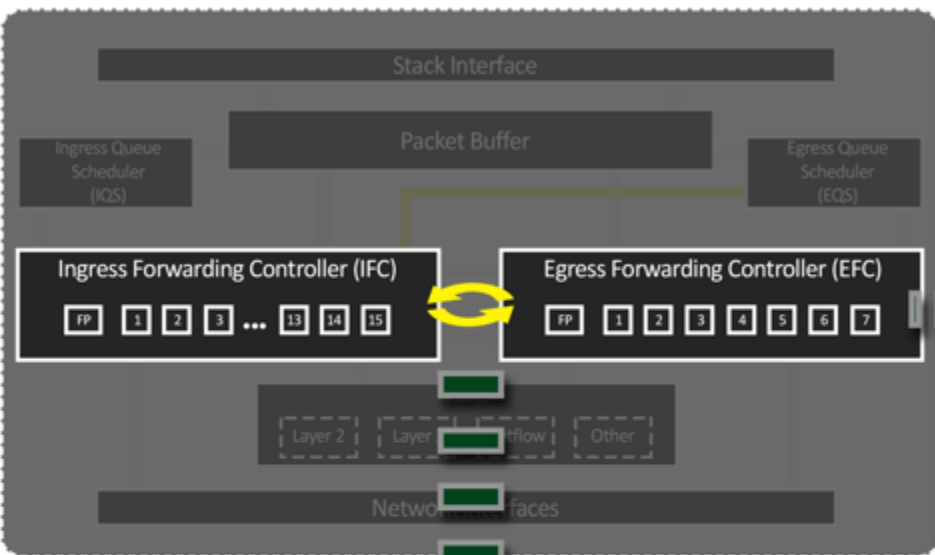
Unified Access Data Plane (UADP) Functional Diagram





All Tables  
On-Chip

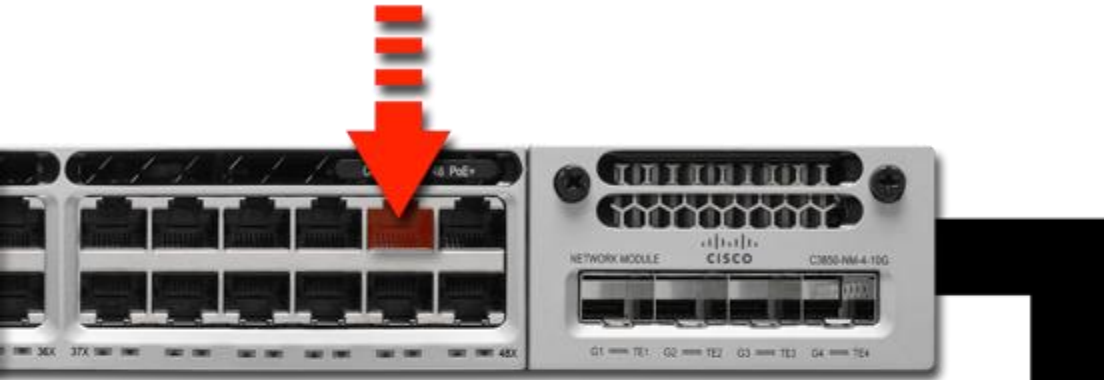
Tb of On-Chip  
Bandwidth



Re-Circulation

Recirculate up to 16 Times

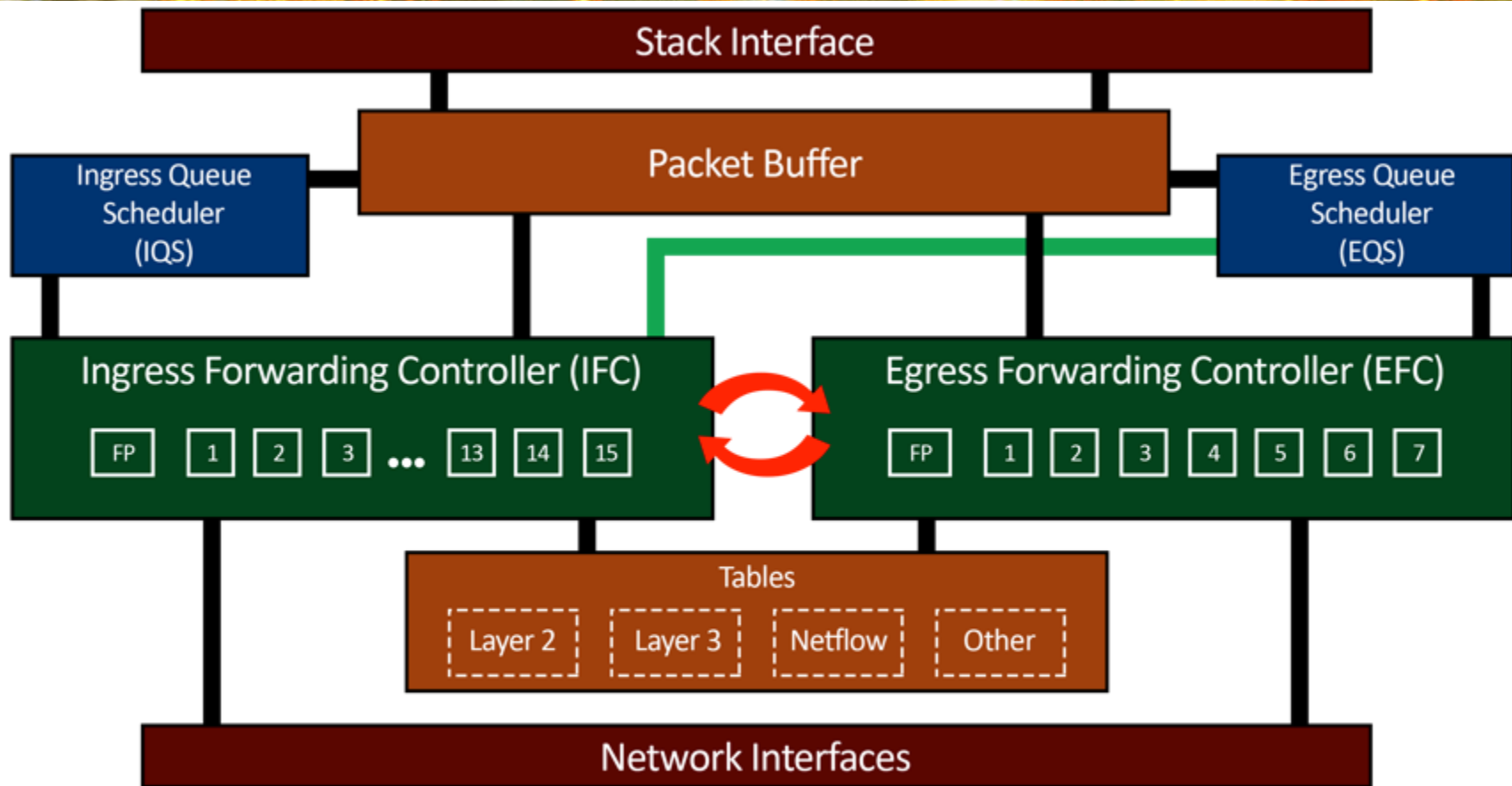
Source



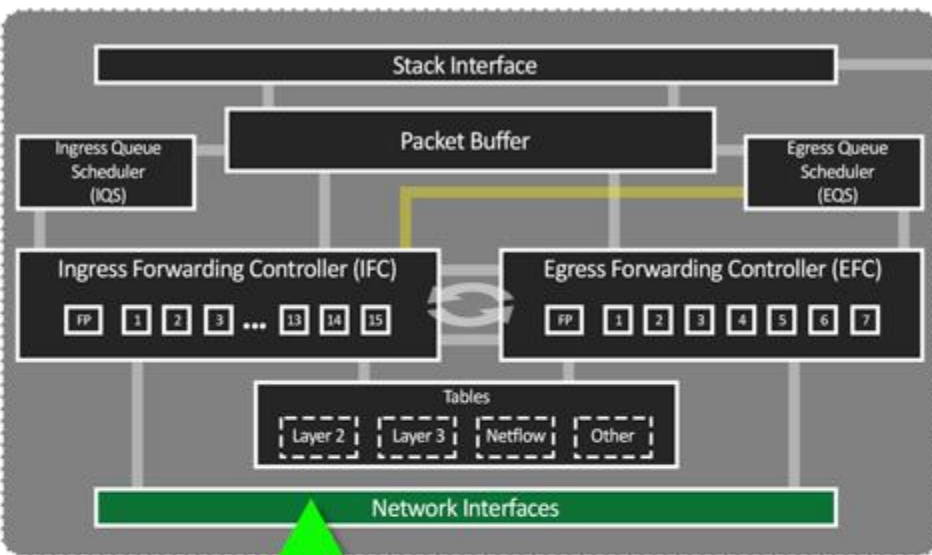
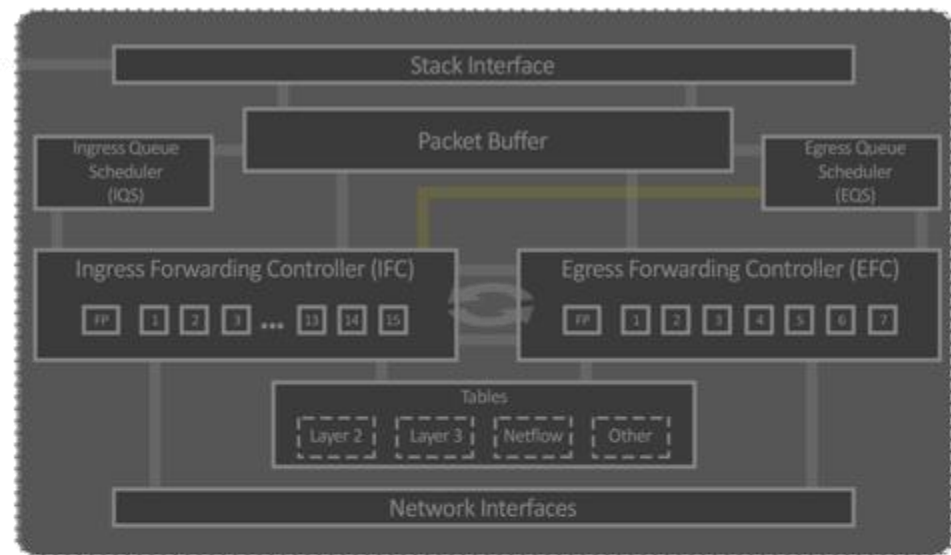
# UADP Packet Walk Scenario

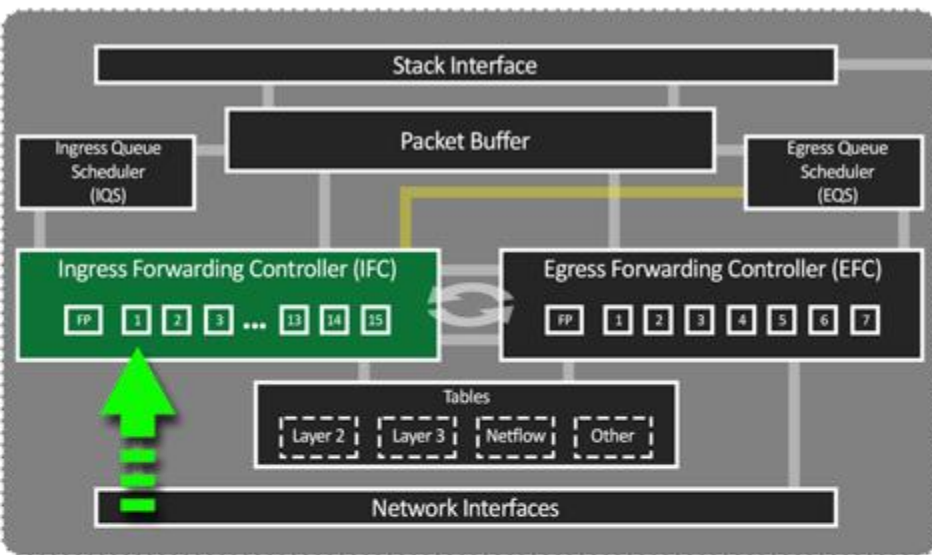
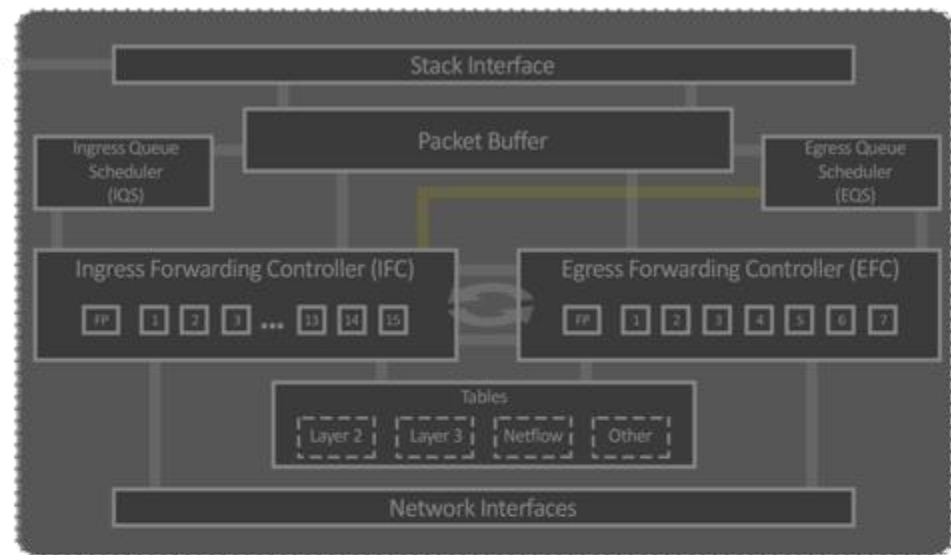


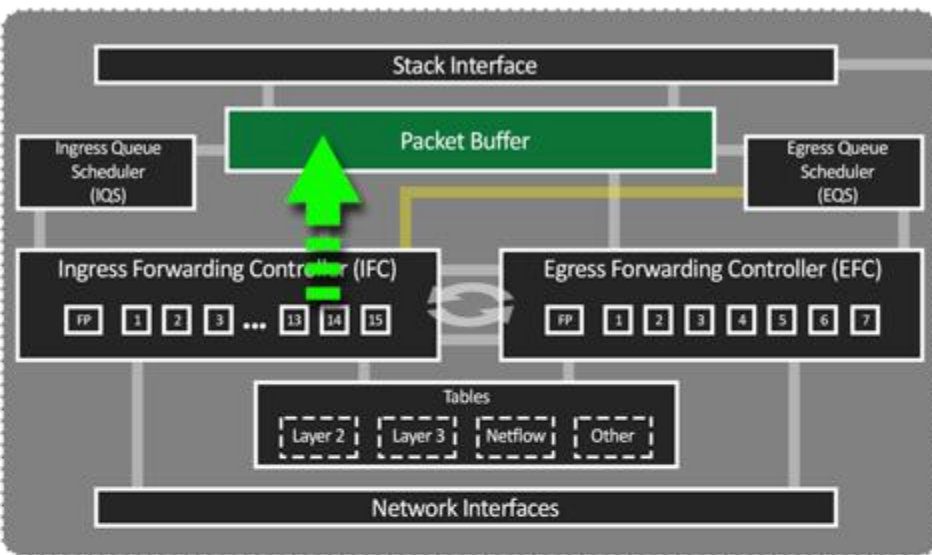
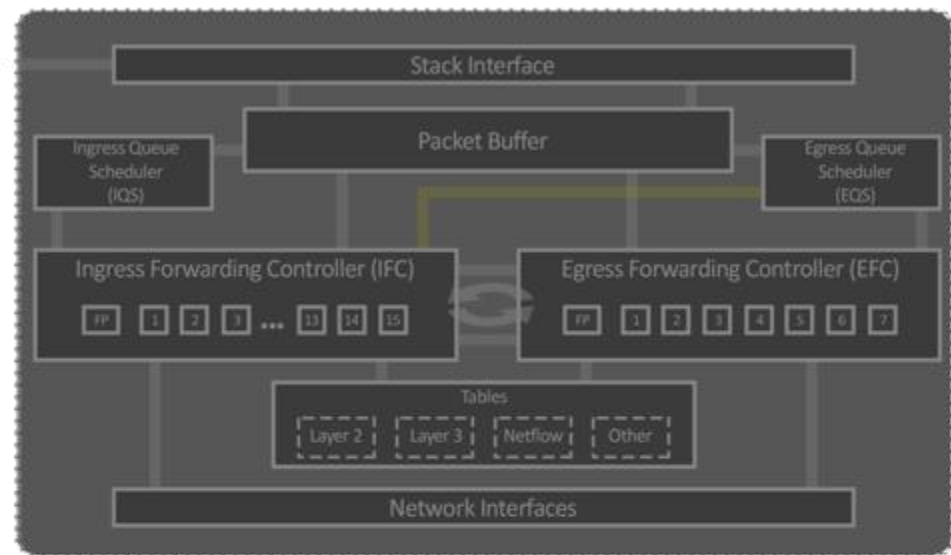
Destination

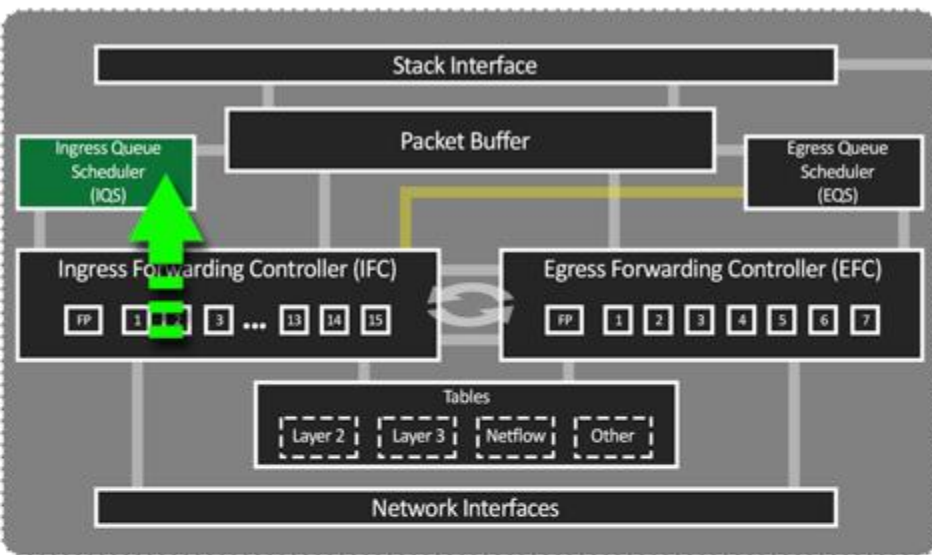
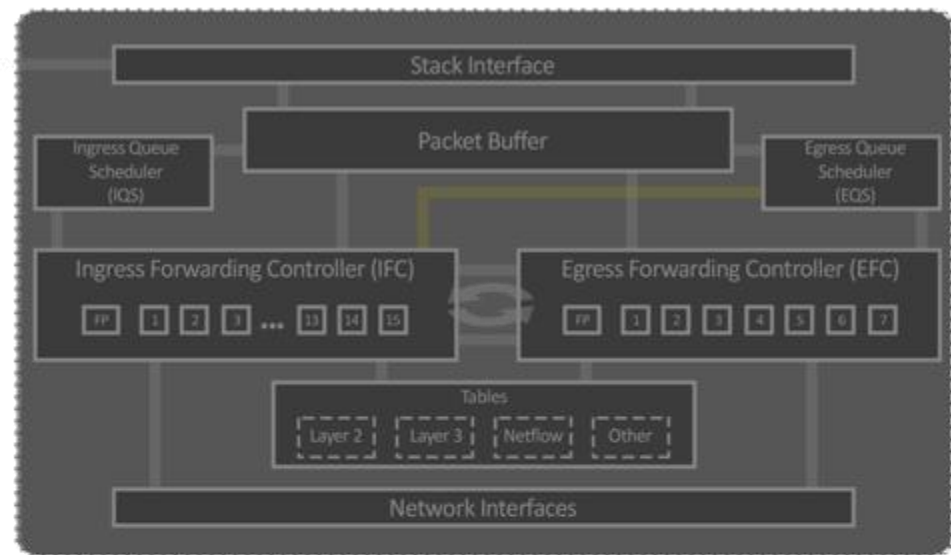


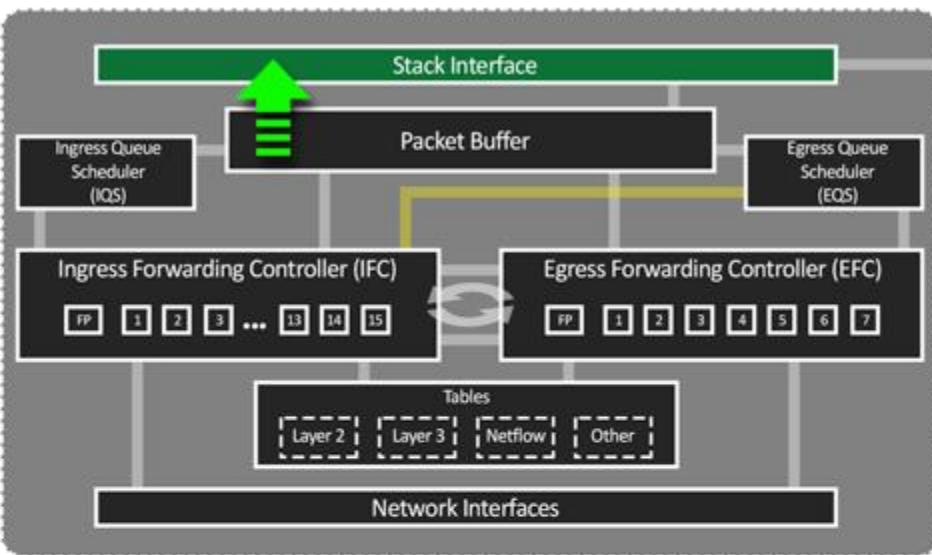
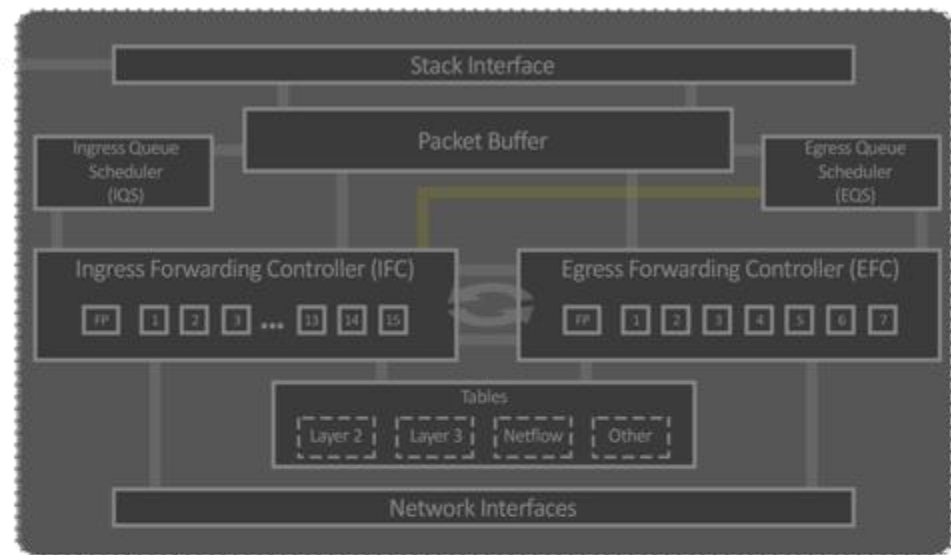
Unified Access Data Plane (UADP) Functional Diagram

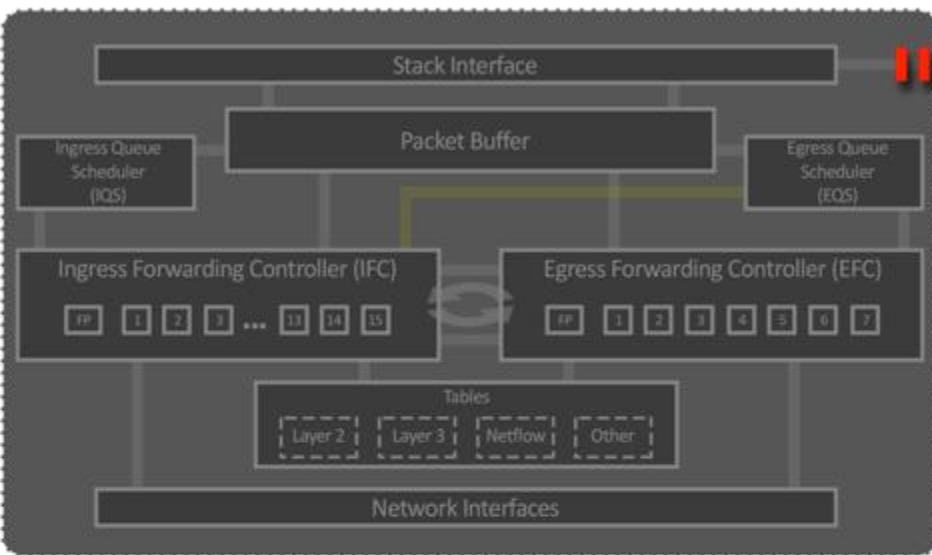
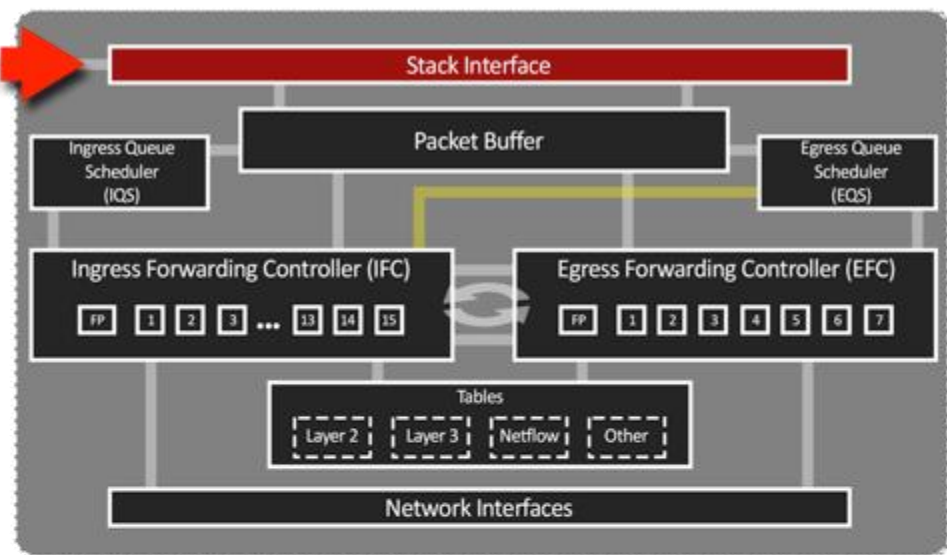


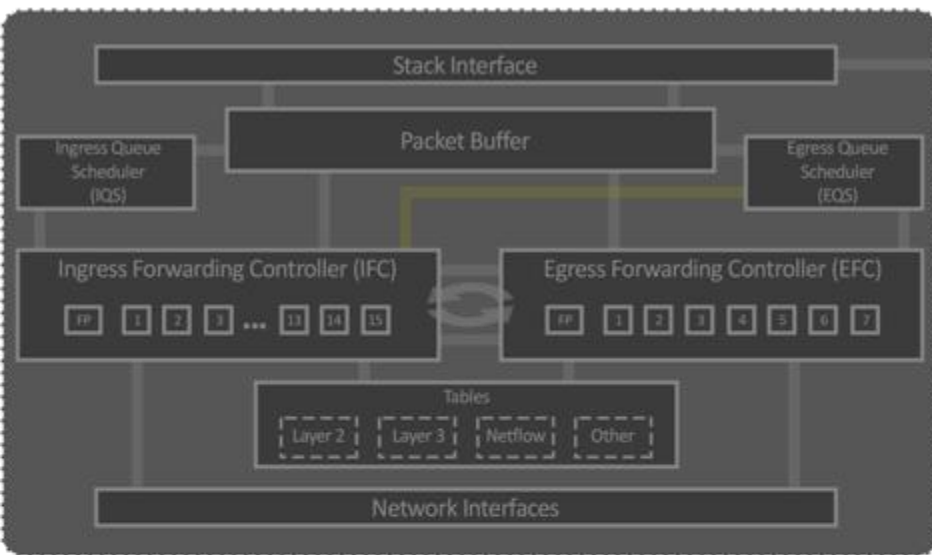
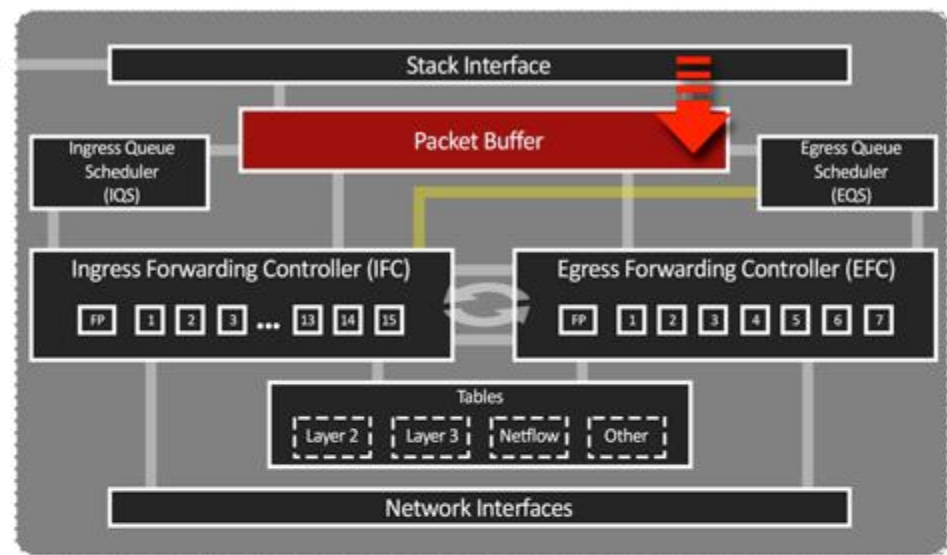


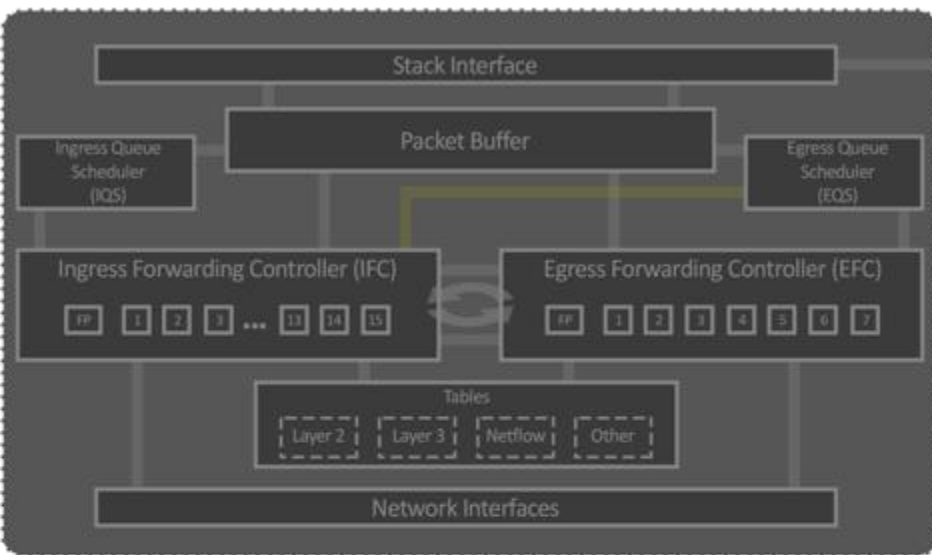
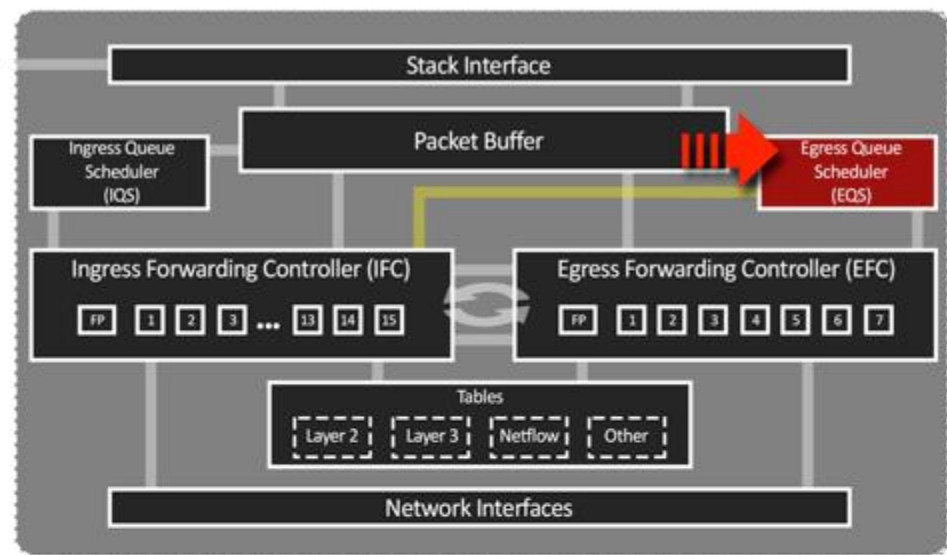


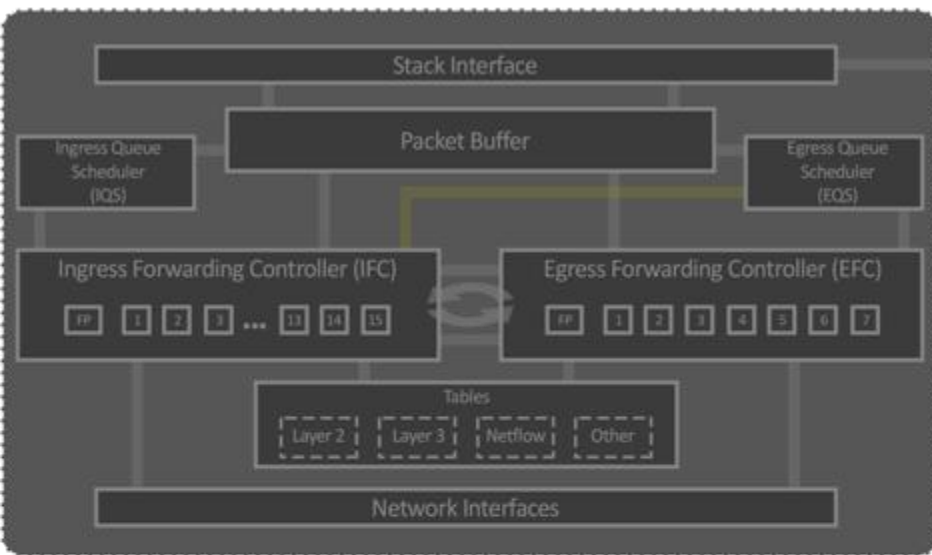
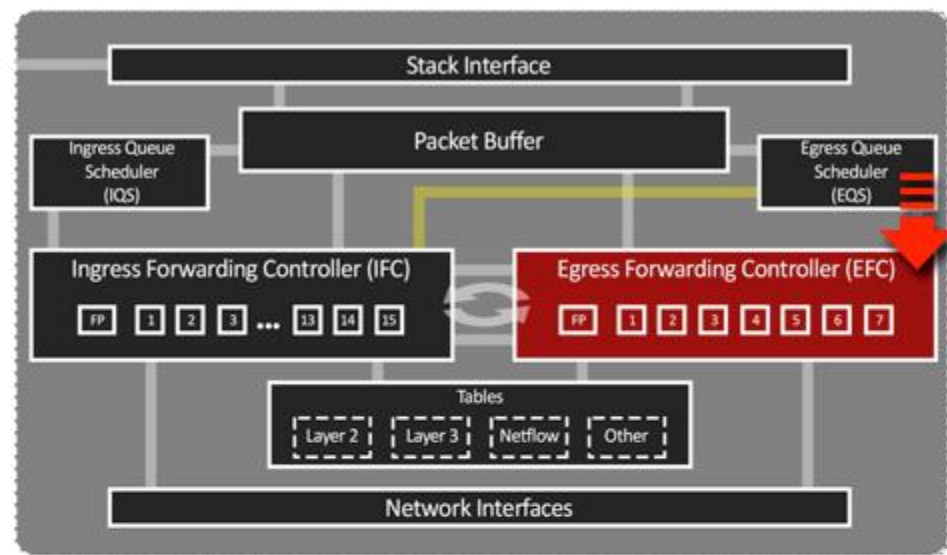


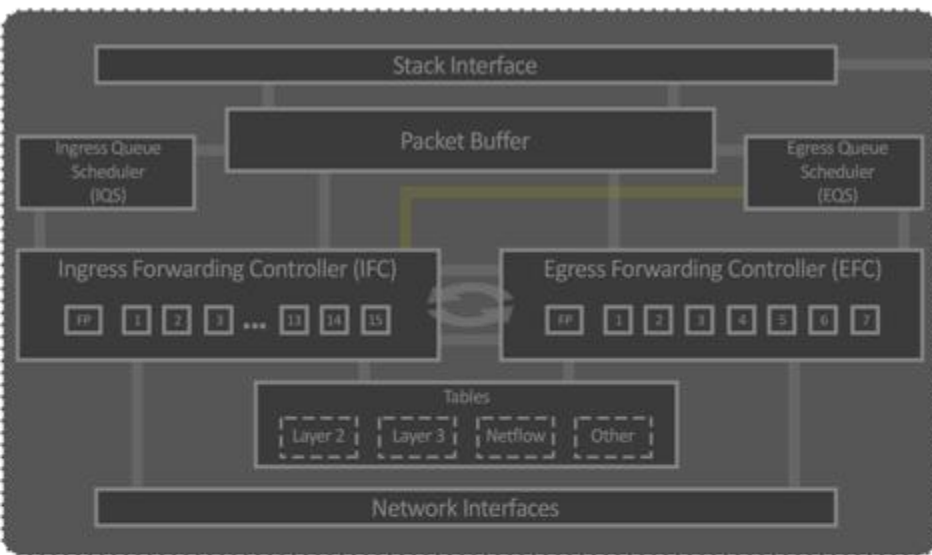
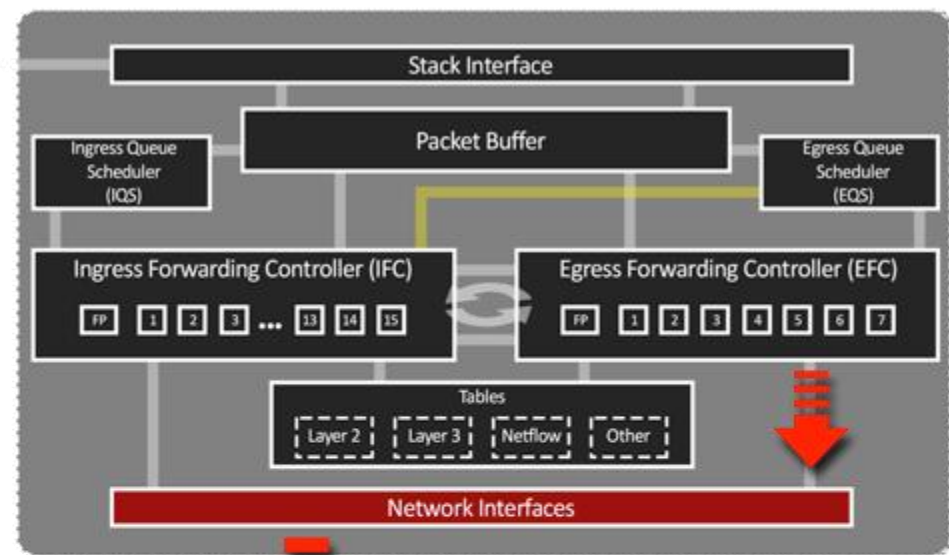


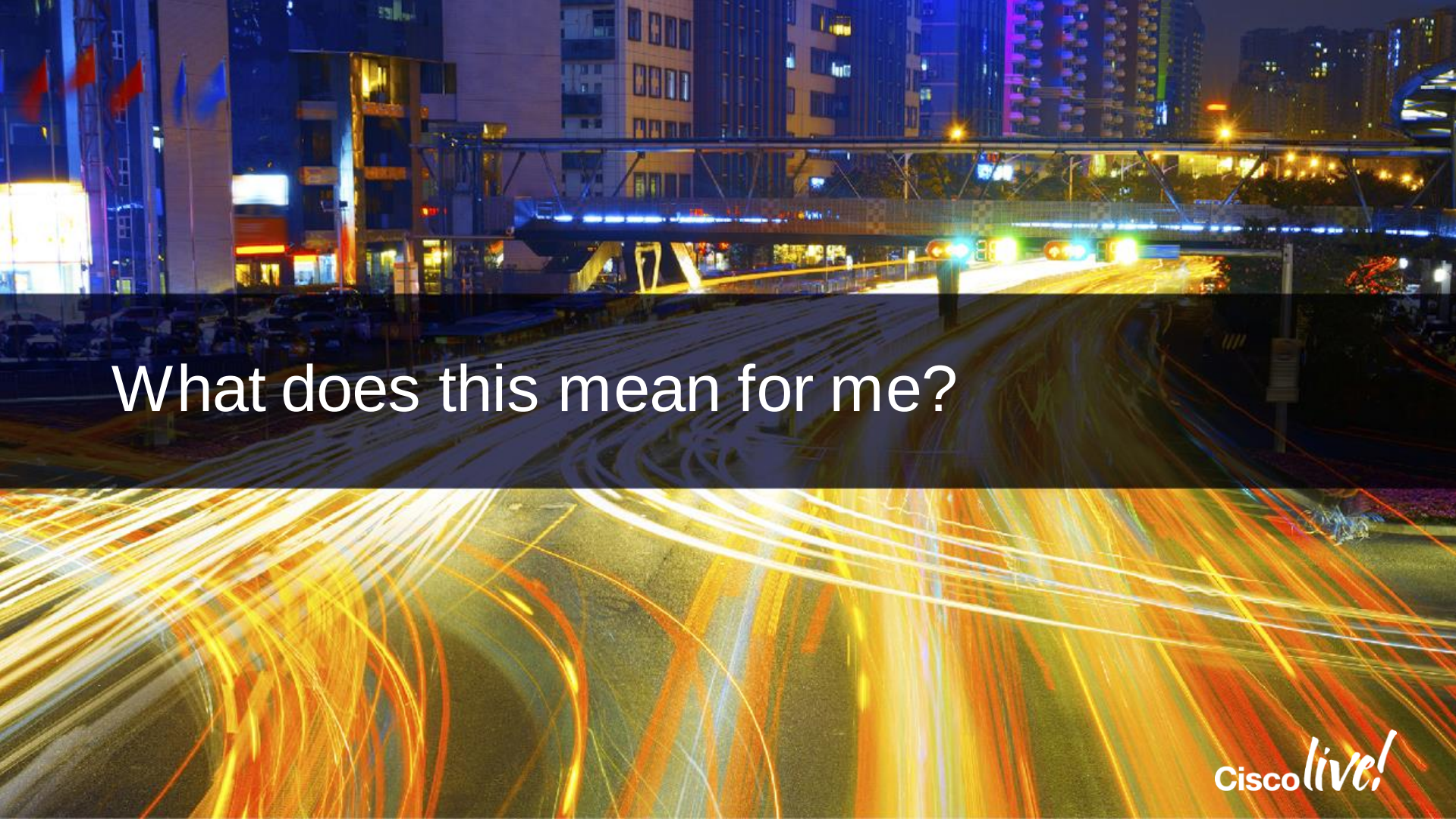












What does this mean for me?

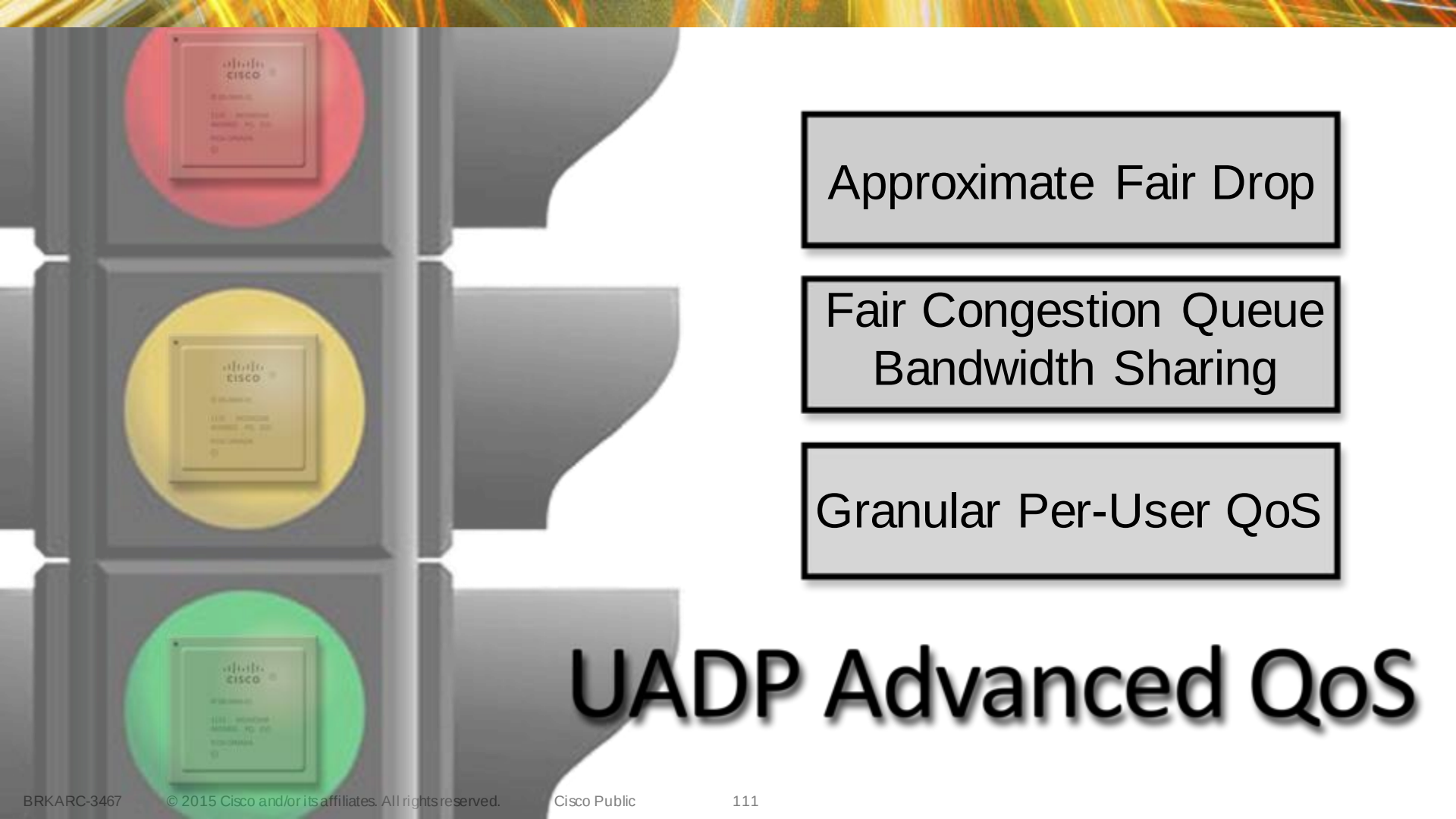


# UADP Programmable Hardware

## equals

### FLEXIBILITY

### INVESTMENT PROTECTION



Approximate Fair Drop

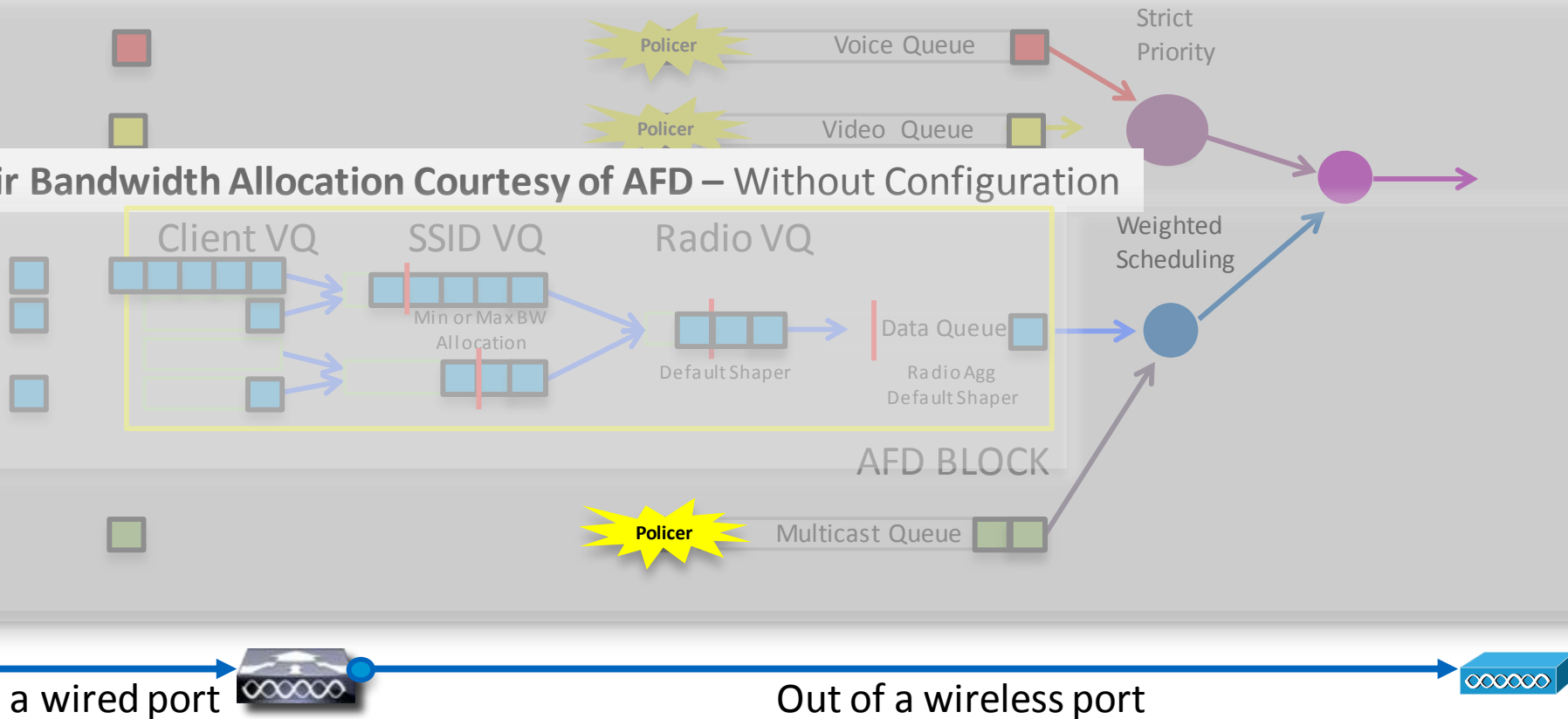
Fair Congestion Queue  
Bandwidth Sharing

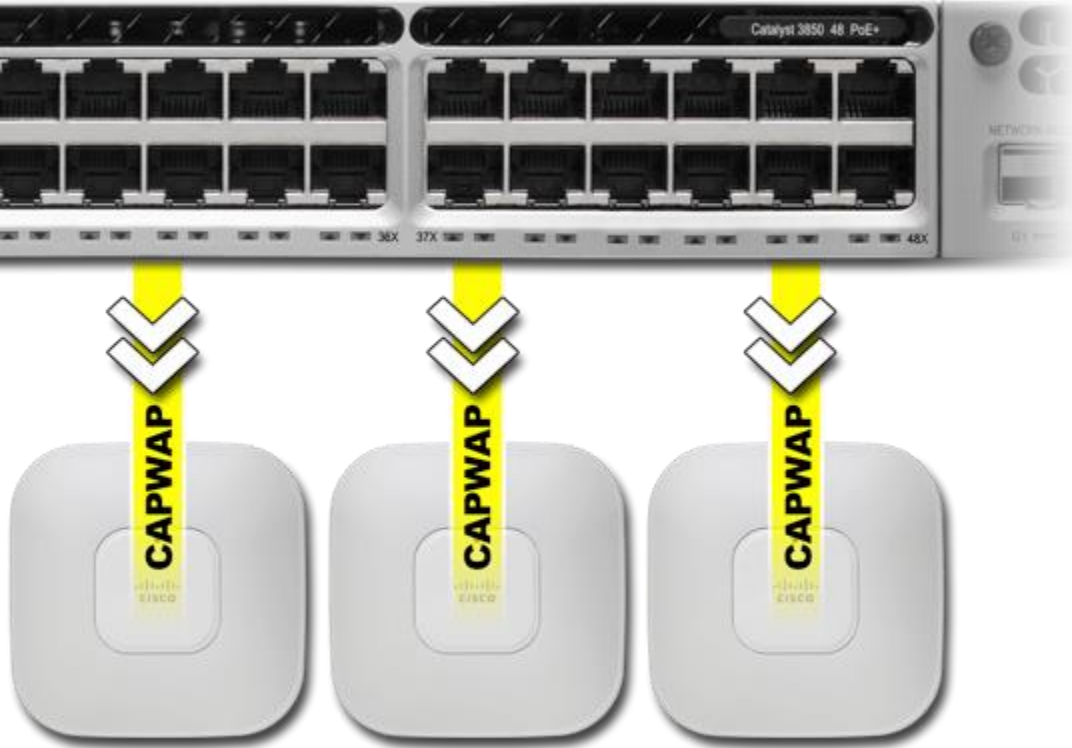
Granular Per-User QoS

# UADP Advanced QoS

# UADP – Approximate Fair Drop

## Fair Bandwidth Allocation Courtesy of AFD – Without Configuration



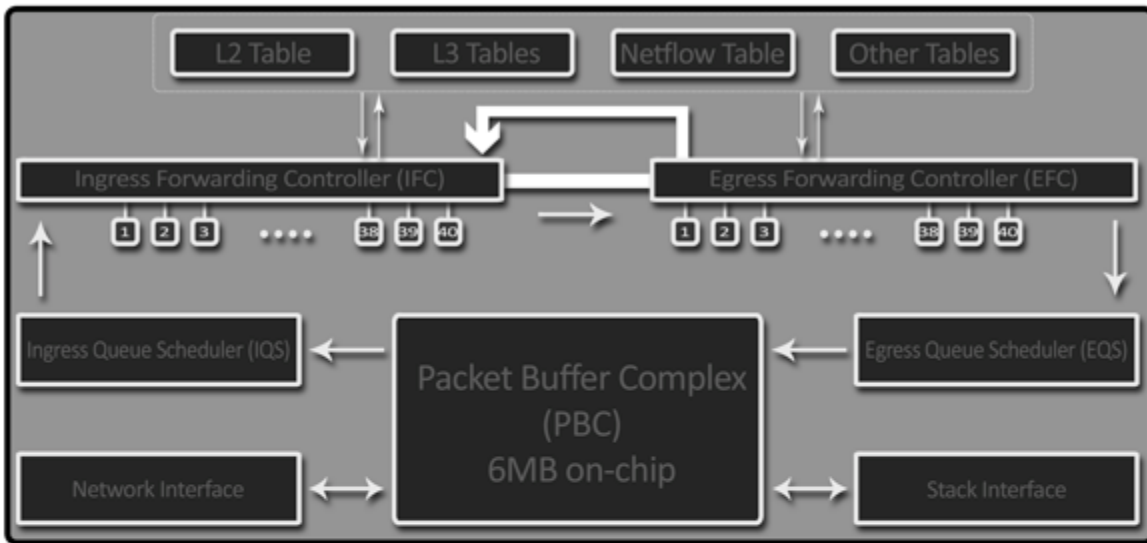


**Traffic Visibility**  
e.g. Netflow

**Control**  
Wired / Wireless QoS / Security

**Scalability**  
802.11ac

# UADP Use Case



**VxLAN\***  
**TRILL\***  
**SPB\***  
**LISP\***  
**and more...**

\* Not Committed



Possible Future UADP Use Cases

*Cisco live!*

WLAN Controller



Catalyst 3650



Catalyst 3850



Catalyst 4500



More to come



# UADP ASIC

Where is it used?

Cisco *live!*

# Why UADP?



Features and Flexibility

Performance

Scalability



# Where Else is Cisco Innovating in Silicon?

## A Few More Enterprise Examples ...



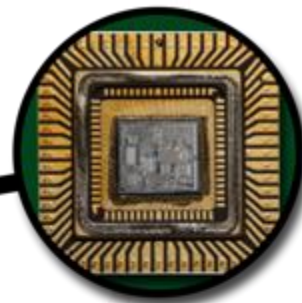
**Monticello**  
Nexus 3548  
Low Latency



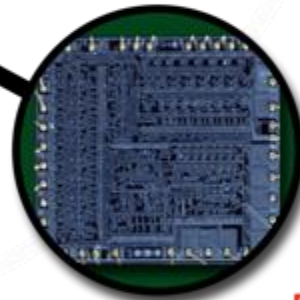
**Big Sur**  
Nexus 6000  
High Density  
10G/40G



**F3 - Nexus 7000/7700**  
DC, 40G/100G



**Raven**  
Cisco 8K/9K  
IP Phones  
Std Video  
Security



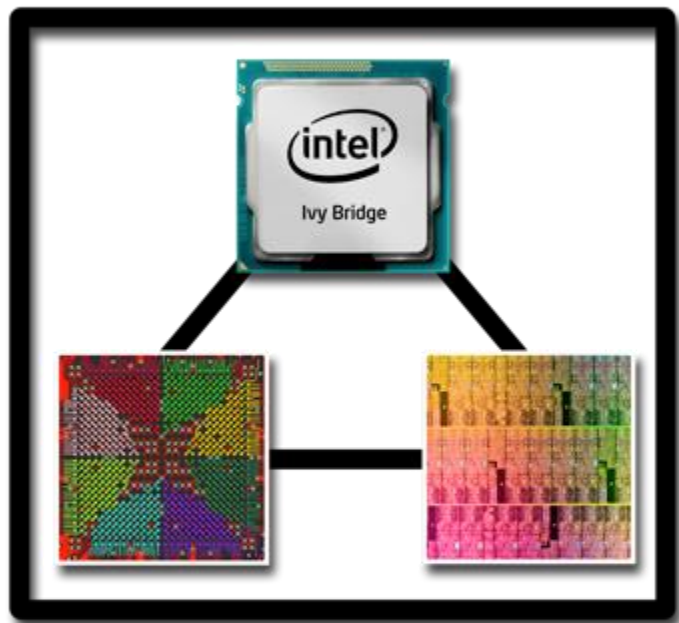
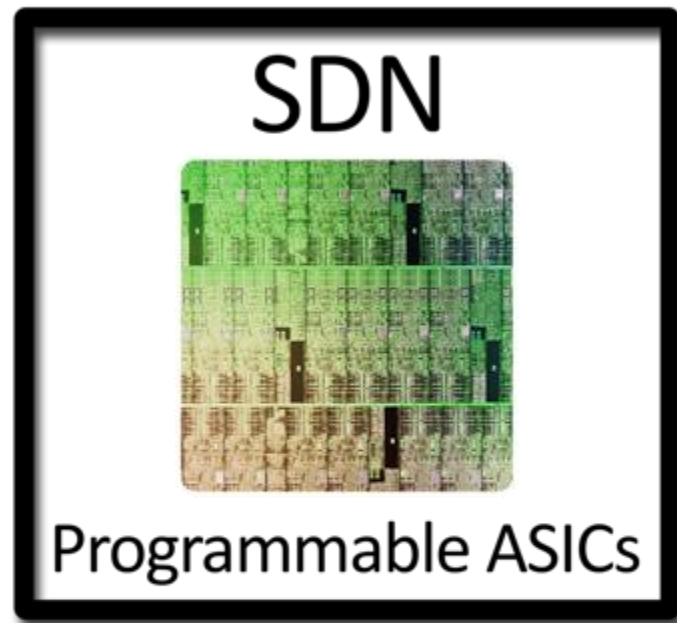
**Psylocke**  
Cisco 7000  
IP Phones  
3rd Party XML Apps

**Cisco** *live!*

# Agenda

- Why ASICs?
- How is an ASIC Developed?
- Merchant vs. Custom
- Cisco ASIC History
- The Move to Programmability
- QFP
- UADP
- Summary





# Trend towards programmability



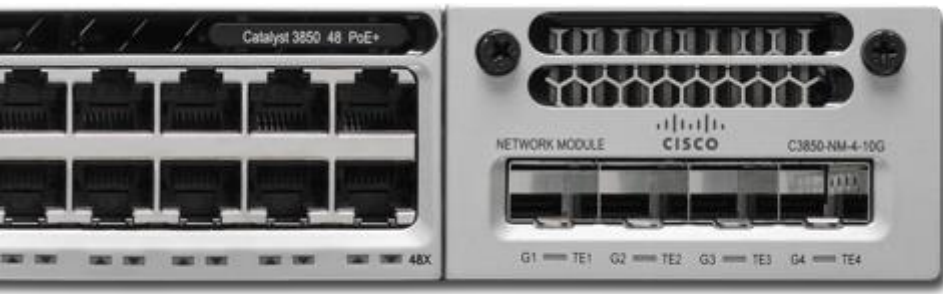
Time to Market

Specific Customer  
Requirements

VS.



Innovation  
Optimisation  
Economies of Scale  
Lead Market  
Deliver Value



# Where ASICs Play...

Network Application Layer

Control Layer

Network Element Layer

# QFP



# UADP



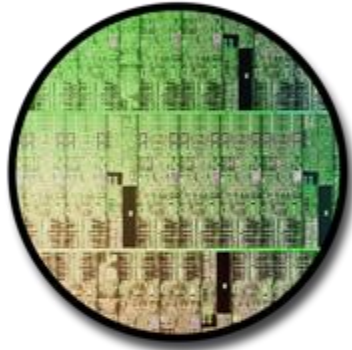
## In-House Developed Programmable Silicon

ASICs

Products

Solutions

Benefits



# Critical Role of ASICs

# Summary

## Did I Achieve My Objective?

Do You Have a Better Understanding ...  
of how **ASICs** are designed and built ...

of the **capabilities** they provide,  
and the **critical role** they play in the network ...

and how they **enable innovation**  
**in network devices and services?**

**Don't Forget**  
to fill out your evaluations!





# Call to Action

- Visit the World of Solutions for
  - Cisco Campus
  - Walk in Labs
- Meet the Expert
- DevNet zone related labs and sessions



Q & A

Cisco *live!*

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